Faculty of Electrical Engineering and Communication
Department of Microelectronics

STEP BY STEP

CADANCE MANUAL AND EXAMPLES

Schematic

Ing. Ahmad Khateb, Ph.D.

Contents

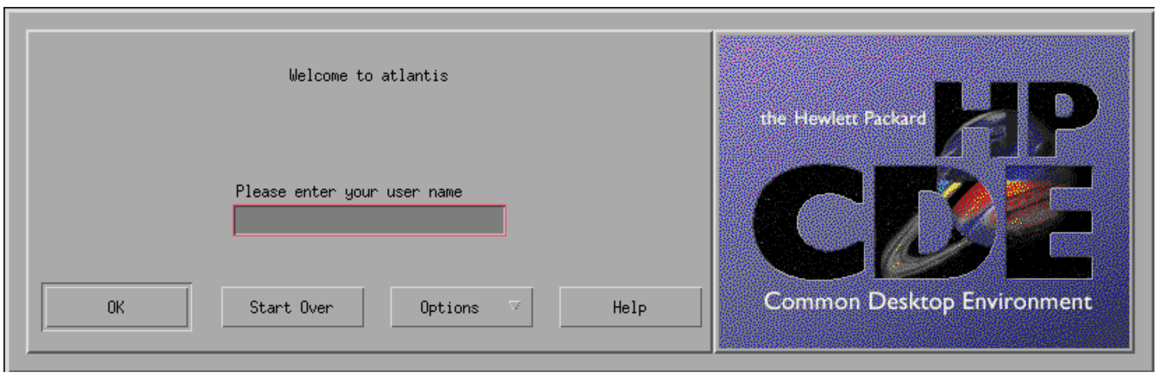
Virtuoso® schematic composer

The Virtuoso® schematic composer is a design entry tool that supports the work of logic and circuit design engineers. Physical layout designers and printed circuit board designers can use the information as background material to support their work.

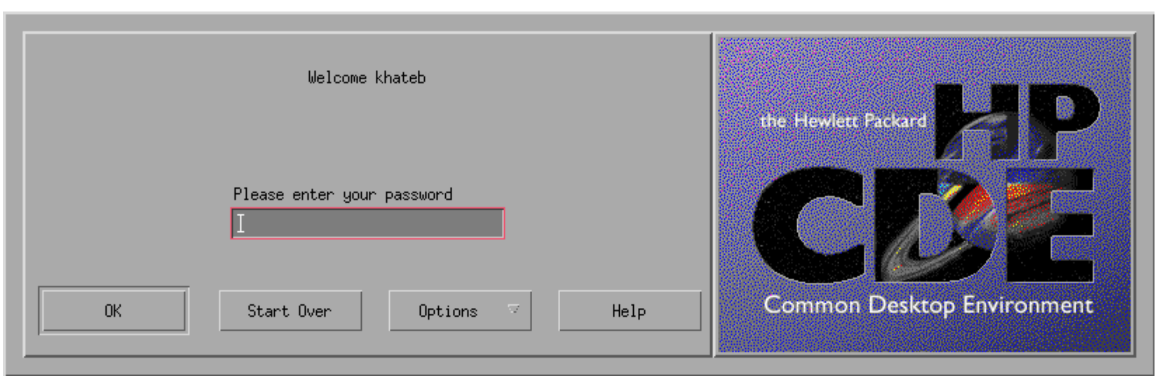
1 Starting Cadence and Making a new Working Library

In order to organize your new circuits, you need to start the **Common Desktop Environment** and create a new library using the Cadence library manager to hold your design files. Carry out the following steps:

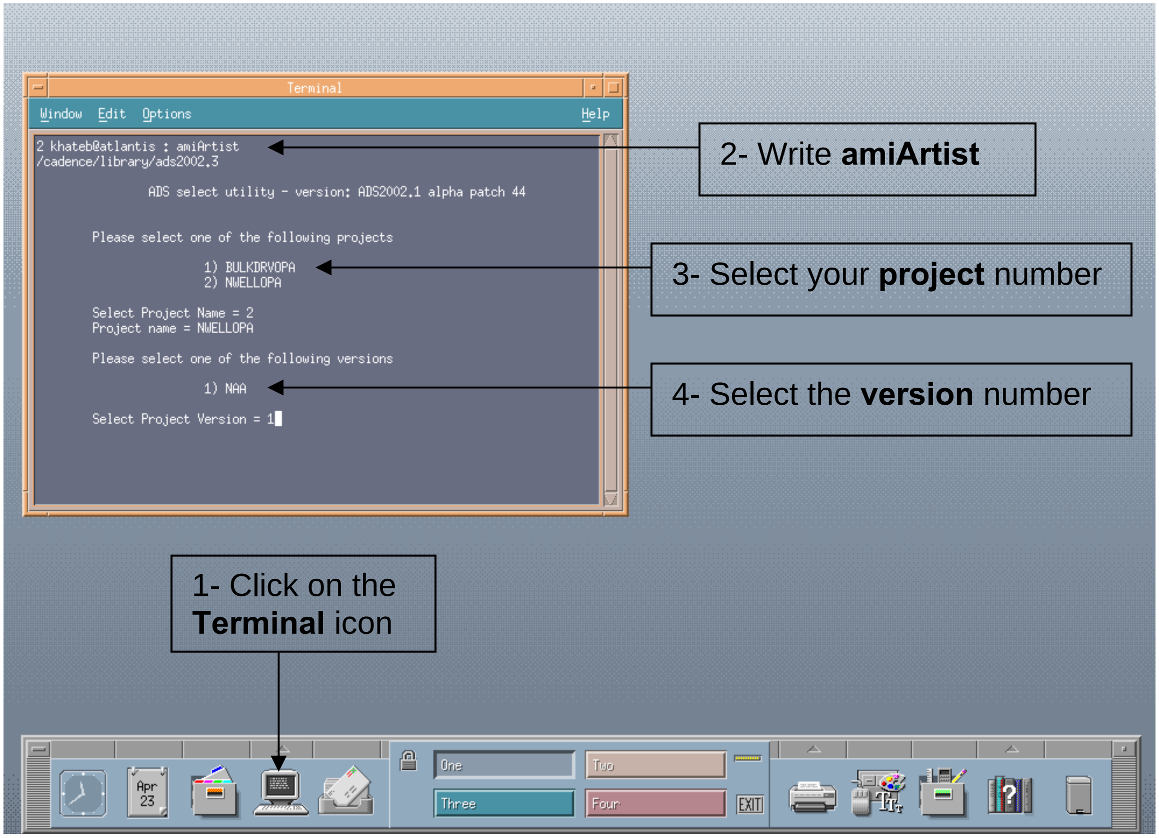
1. Enter your user name



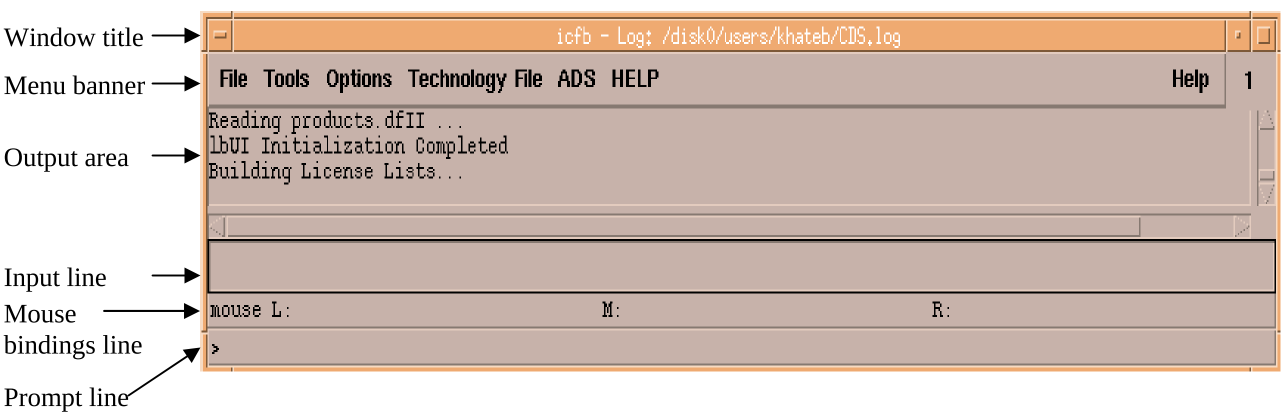
2. Enter your password



3. **Common Desktop Environment** will appear
    1. Click on the terminal icon
    2. Write amiArtist then click Enter
    3. Select your project number then click Enter
    4. Select the version number then click Enter



4. Click Enter then you should get a window (called the **Command Information Window - CIW**). The CIW is the control window for the Cadence software. The following figure shows the parts of the CIW.



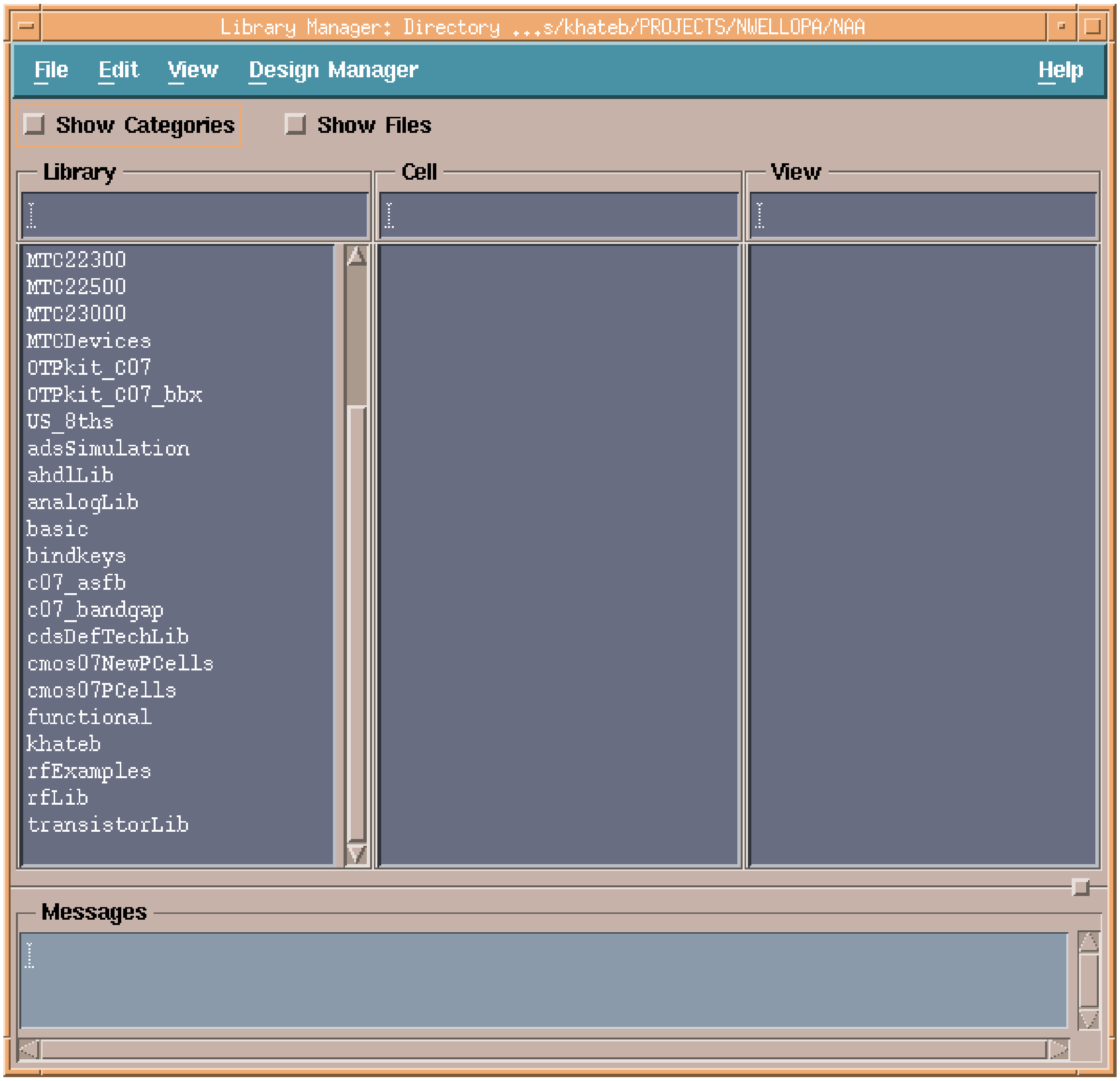
- **Window title** displays the Cadence executable name and the path to the log file that records your current editing session. The log file appears in your home directory.
- **Menu banner** lets you display command menus to access all the Cadence design framework II tools.
- **Output area** displays a running history of the commands you execute and their results. For example, it displays a status message when you open a library. The area enlarges when you enlarge the CIW vertically.
- **Input line** is where you type in Cadence SKILL language expressions or type numeric values for commands instead of clicking on points.
- **Mouse bindings line** displays the current mouse button settings. These settings change as you move the mouse in and out of windows and start and stop commands.
- **Prompt line** reminds you of the next step during a command.

Recommendation:

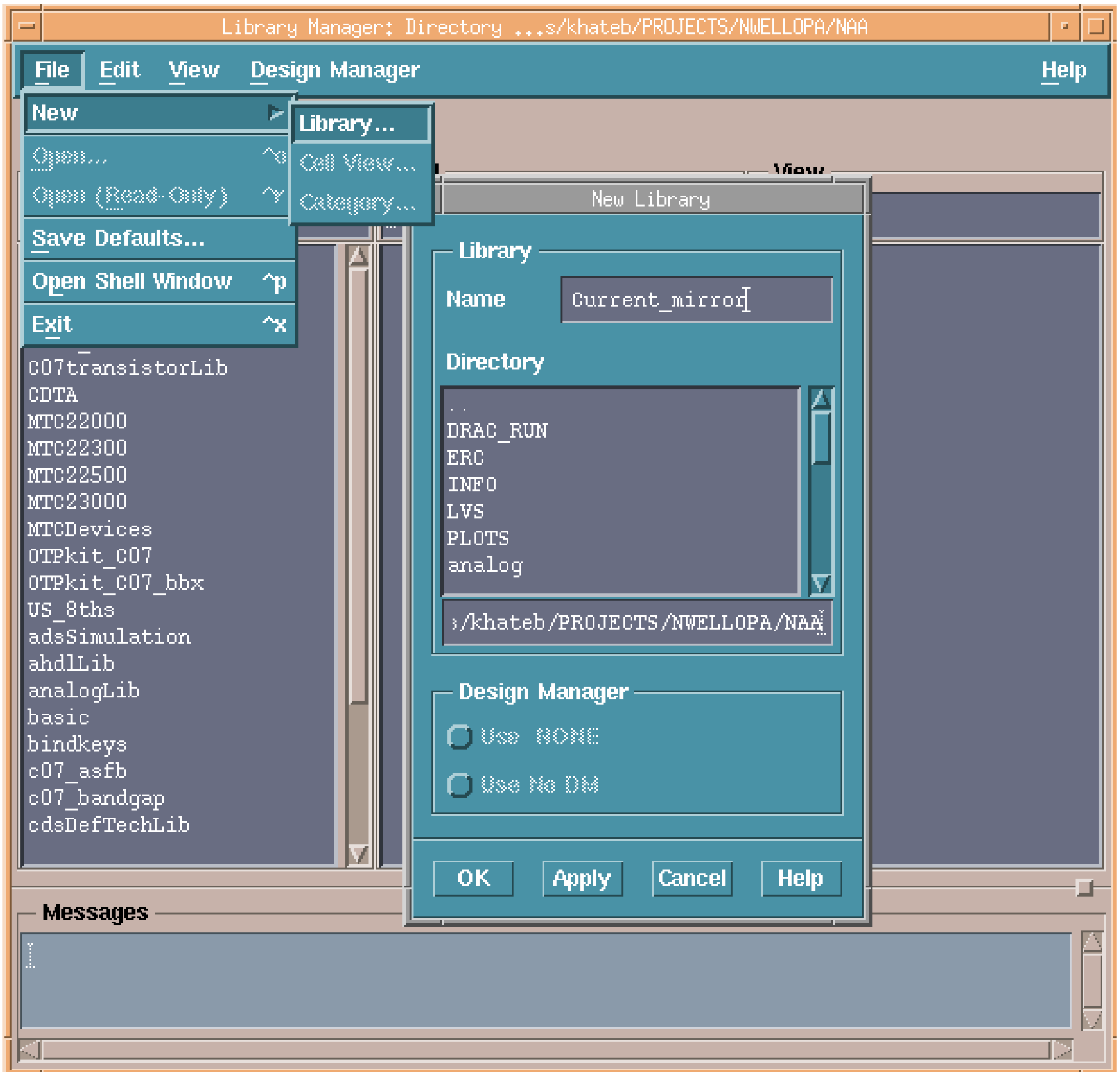
Keep the **Command Information Window - CIW** in sight, from the **CIW**, you can access all Cadence tolls and functionalities

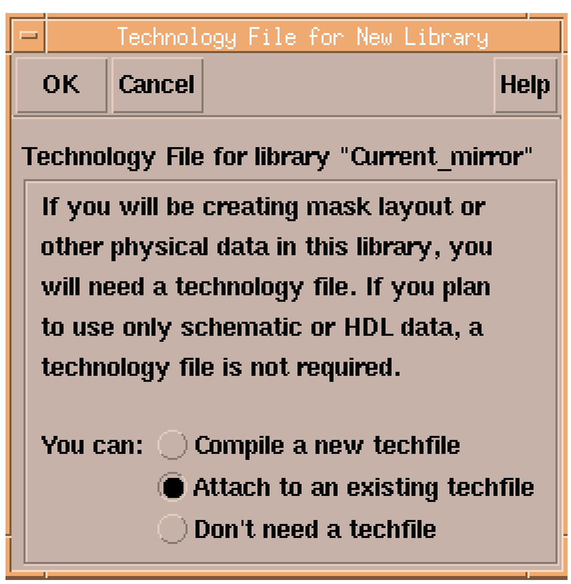
- view prompts,
- view error and informational messages,
- start specific tools,
- run SKILL command

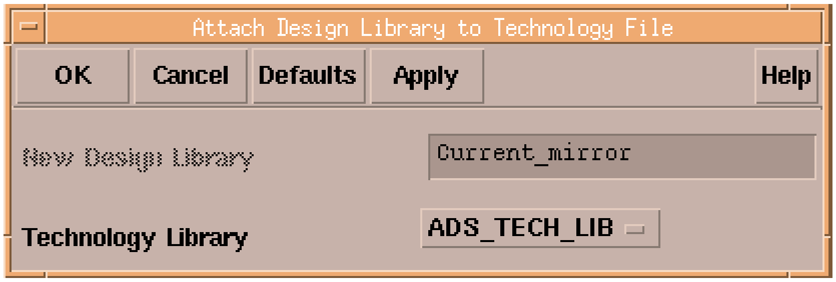
5. Library Manager will automatically be opened. If not, in the CIW, select **Tools** → **Library Manager...** You should get the following window, with the following list of libraries.



3. In order to build your own schematics, you'll need to define your own library to keep your own circuits in. To create a new working library in the library manager, select **File** → **New** → **Library**. In the Create Library window that appears fill in the Name field as Current_mirror (or whatever you'd like to call your library) then click **Apply**, a "**Technology File for New Library**" appear, select "**Attach to an existing techfile**" then click **OK.** Select the **ADS_TECH_LIB** from Technology Library and press **OK**.


Library Manager: Directory ...s/khateb/PROJECTS/NWELLOPA/NAA
File
Edit
View
Design Manager
Help
New
Library...
Cell View...
Category...
Open...
Open (Read-Only)
Save Defaults...
Open Shell Window ^p
Exit ^x
C07transistorLib
CDTA
MTC22000
MTC22300
MTC22500
MTC23000
MTCDevices
OTPkit_C07
OTPkit_C07_bbx
US_8ths
adsSimulation
ahdlLib
analogLib
basic
bindkeys
c07_asfb
c07_bandgap
cdsDefTechLib
View
New Library
Library
Name
Current_mirror
Directory
..
DRAC_RUN
ERC
INFO
LVS
PLOTS
analog
s/khateb/PROJECTS/NWELLOPA/NAA
Design Manager
Use NONE
Use No DM
OK
Apply
Cancel
Help
Messages


Technology File for New Library
OK
Cancel
Help
Technology File for library "Current_mirror"
If you will be creating mask layout or
other physical data in this library, you
will need a technology file. If you plan
to use only schematic or HDL data, a
technology file is not required.
You can:
Compile a new techfile
Attach to an existing techfile
Don't need a techfile



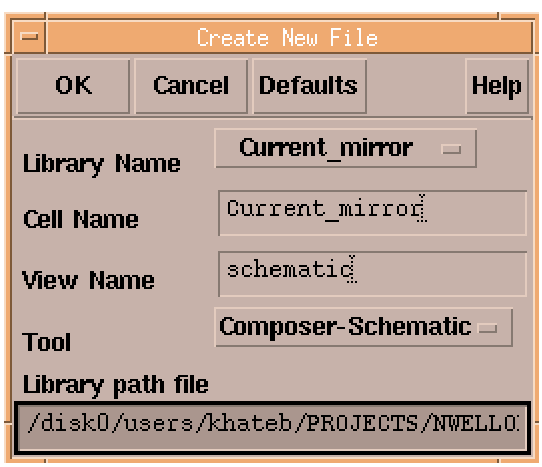
Now the working library has been created. All the project cells (components) that you generate should end up in this library. When you start up the Library Manager to begin working on your circuits, make sure you select your own library to work in.

2 Creating a New Cell

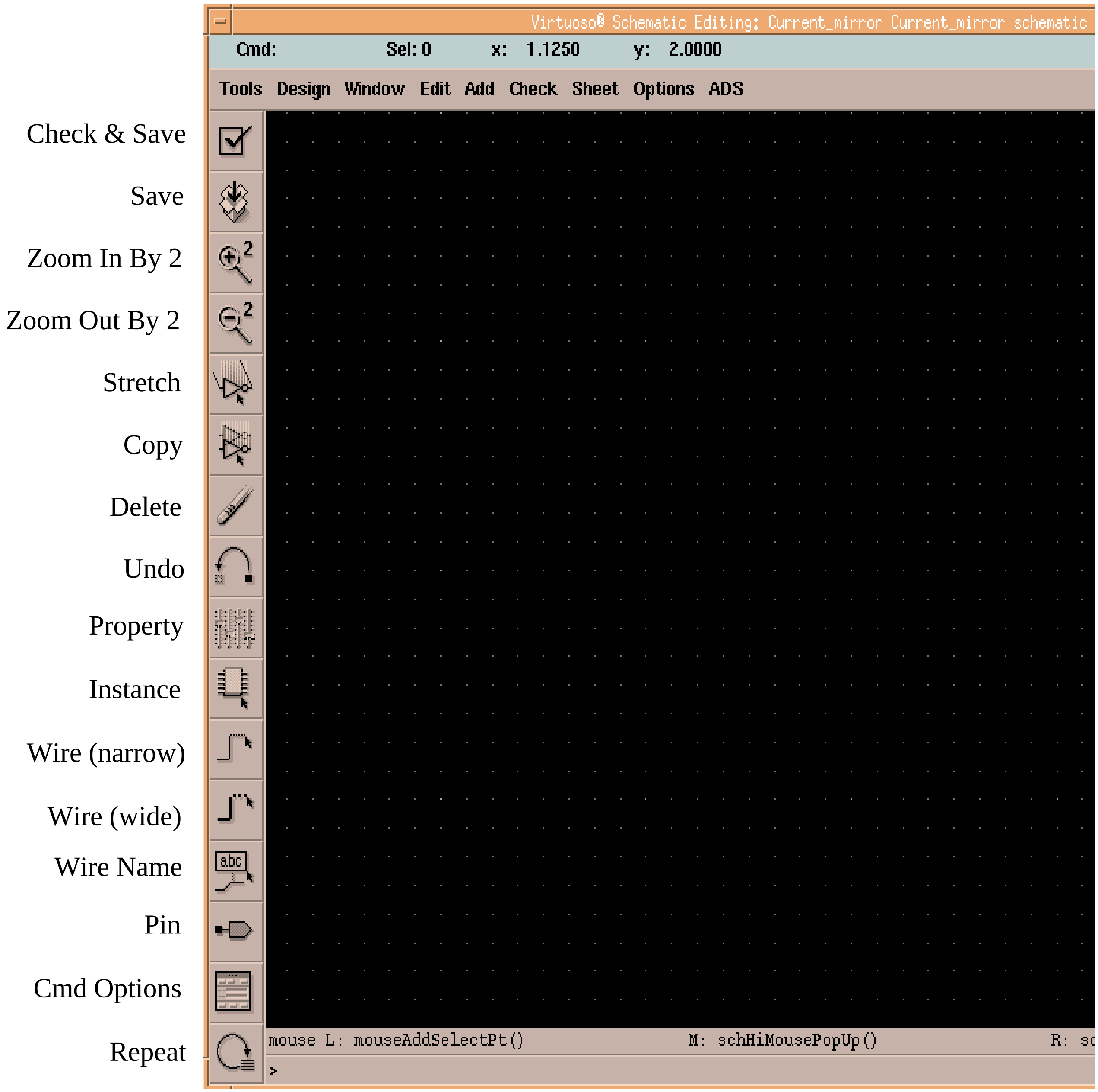
When you create a new cell (component in the library), you actually create a view of the cell. For now we'll be creating "schematic" views, but eventually you'll have other different views of the same cell. For example a "layout" view of the same cell will have the composite layout information in it. It's a different file, but it should represent the same circuit. This will be discussed later in more details. For now, we're creating a schematic view. To create a cell view, carry out the following steps:

2.1 Creating the Schematic View of an Current_mirror

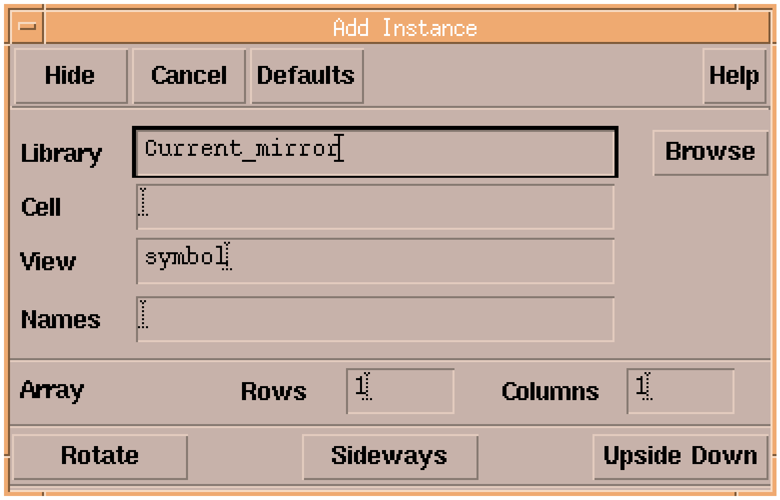
1. Select **File** → **New** → **Cell View...** from the Library Manager menu or to the CIW menu. The Create New File window appears. The Library Name field is **Current_mirror**. Fill in the Cell Name field as **Current_mirror**. Choose **Composer-Schematic** from the Tool list and the view name is automatically filled as **Schematic**. The library path file is automatically set. Click **OK**.



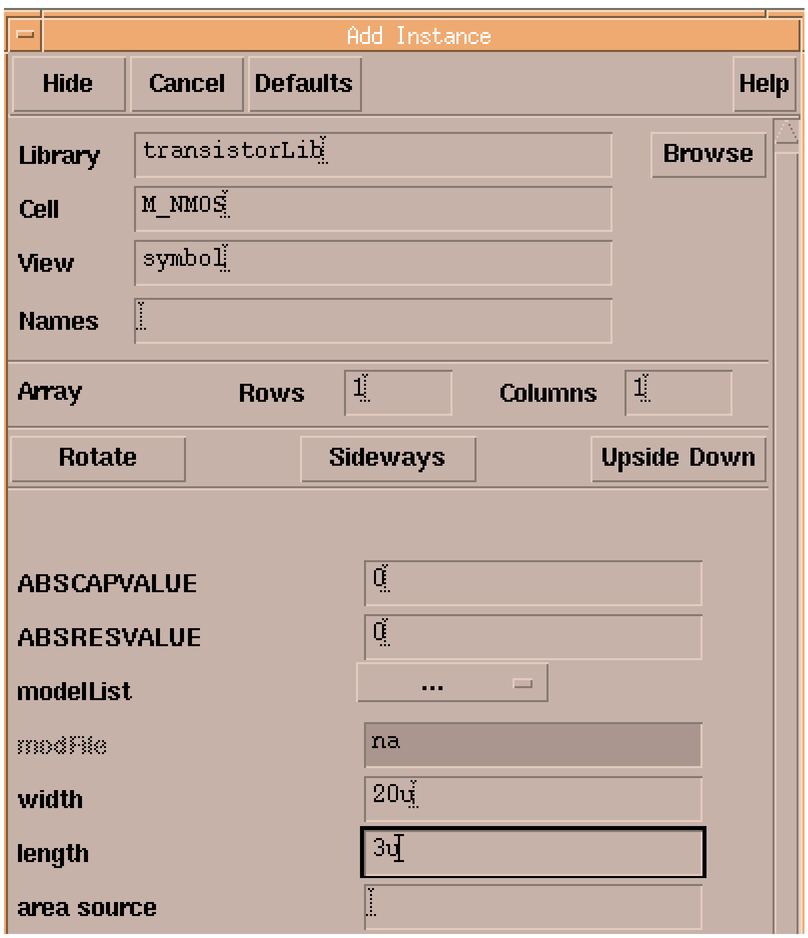
2. A blank window called **Virtuoso Schematic Editing: Current_mirror Current_mirror** Schematic appears.



3. Adding Instances: An instance (either a gate from the standard cell library or a cell that you've designed earlier) can be placed in the schematic by selecting **Add → Instance... or by pressing "i"**, and the following **Add Instance window** appears.



4. For this example, we need to add the following components: two identical NMOS transistors of W/L= 20/3 um and one resistor of 15K ohm. To add the NMOS transistors, press **Browse** then select the **transistorLib Library** → **M_NMOS Cell** → **symbol View**, This opens the **Add Instance** window



Now, enter the M_NMOS transistor value of W/L= 20/3 um and hit **Hide**. Place the first M_NMOS in the schematic window then press "**G**" key from the keyboard for "Horizontal Mirror" of the second M_NMOS. Other instances can be added in the similar fashion as above.

To come out of the instance command mode, press **Esc**. (This is a good command to know about in general. Whenever you want to exit an editing mode that you're in, use **Esc**.

Recommendation:

Hit a bunch of **Esc's** whenever you are not doing something else just to make sure you don't still in a strange mode from the last command.

5. Command Functions

Some common command modes and functions are available under **Add** and **Edit** menus, the most used command are mentioned in the following table:

Keyboard shortcut	Function	Remark
I	Instance	to add instance to schematic
Q	Property	select the instance you want to edit first
W	Wire	
M	Move	select the instance you want to move first
C	Copy	select the instance you want to copy first
G	Mirror ↕	select the instance, press **M** first then **G**
Shift + G	Mirror ↔	select the instance, press **M** first then **G**
Ctrl + W	Rotate	select the instance, press **M** first then **G**
P	Pin	
A	Select	
Ctrl + A	Select All	
D	Deselect	
Ctrl + D	Deselect All	
U	Undo	
Shift + U	Redo	
F	Fit	
Z	Zoom in	

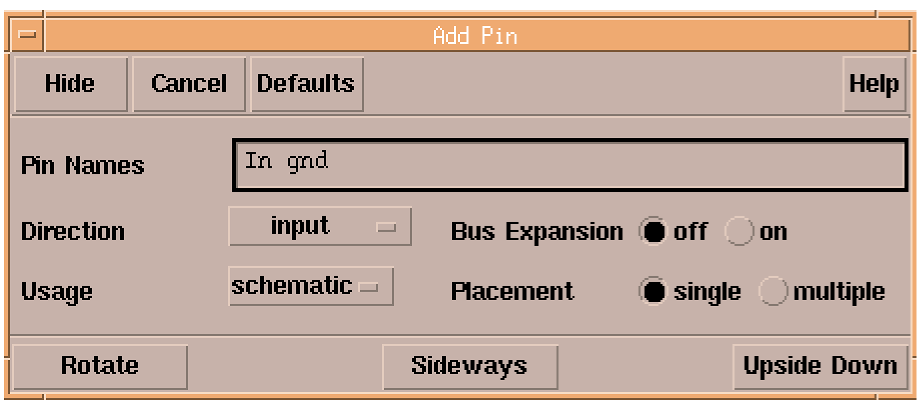
Shift + X	Zoom out	
Shift + S	Check and Save	
S	Stretch	select the instance or wire first then **S**
N	gravity	
V	Edit in place	To edit the symbol in place or to see the internal schematic of the symbol
Ctrl + X	return	

6. Connecting Instances with Wires

To connect the different instances with wires we select **Add** → **Wire (narrow)** or **press "w"** to activate the wire command. Now go to the node of the instance and left-click on it to draw the wire and left-click on another node to make the connection. If you need to end the wire at any point other than a node (i.e. to add a pin later on), double left-click at that point. To come out of the wire command mode, press **Esc**.

7. Adding Pins

Pins can be added by going to **Add** → **Pin… or pressing "p"** For example, to put two input pins In & gnd, we can fill in the **Pin Names** field as **In gnd** (with a space) and the **Direction** list as **input**.



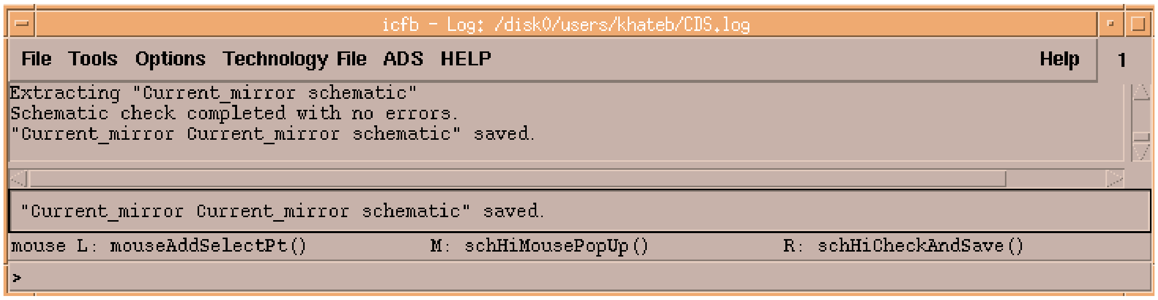
Now go to the wire where you need to place the pin and left-click on it.
Also, add the **output** pin **'Out'** in a similar way.

8. Checking and Saving the Design

The design can be checked and saved by selecting **Design** → **Check and Save**. For an error free schematic, you should get the following message in the **CIW**,

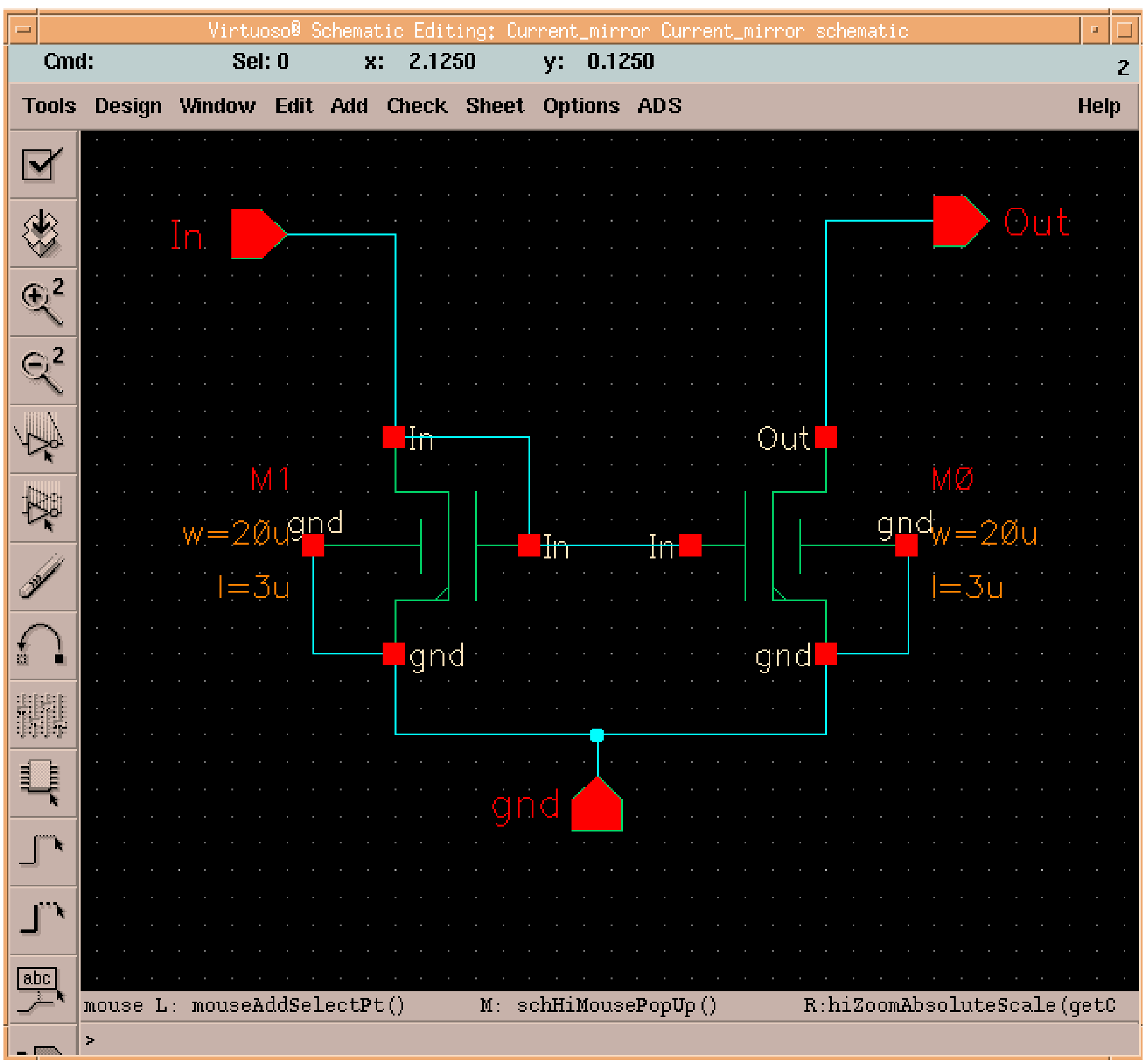
Extracting "Current_mirror schematic"

Schematic check completed with no errors.
"Current_mirror Current_mirror schematic" saved.



Note: The **CIW** should not show any warnings or errors when you check and save.

9. Using all the commands given above the schematic of a Current_mirror can be constructed as shown below.

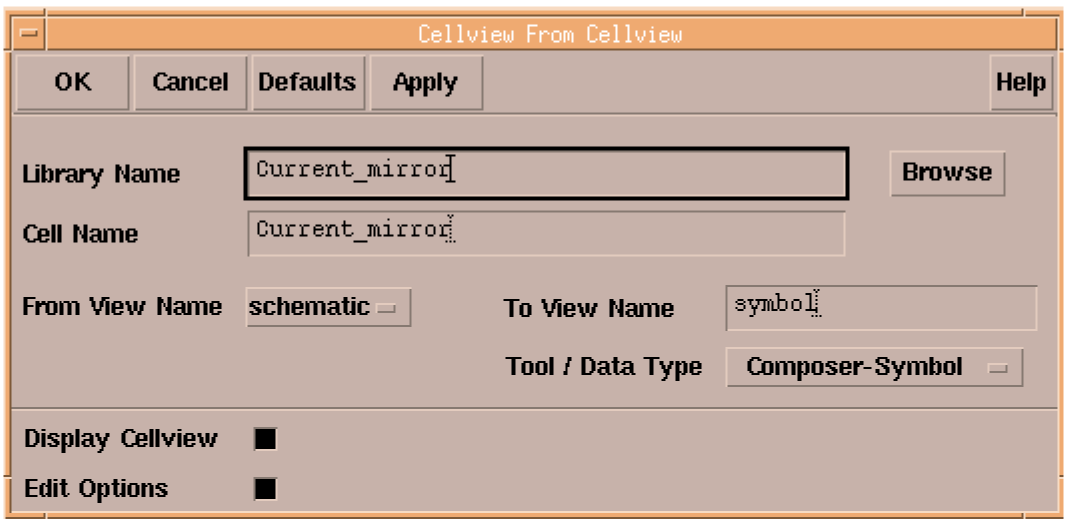


10. After saving the design with no errors, select **Window** → **Close**.

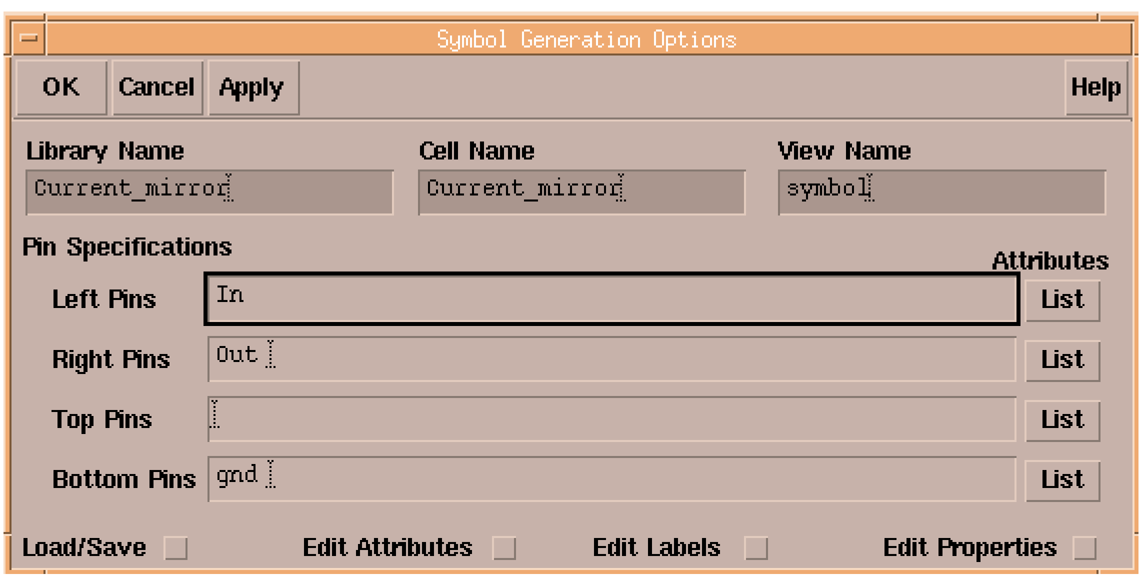
2.2 Creating a Symbol View of the Current_mirror

You have now created a *schematic* view of your Current_mirror. Now you need to create a symbol view if you want to use that circuit in a different schematic.

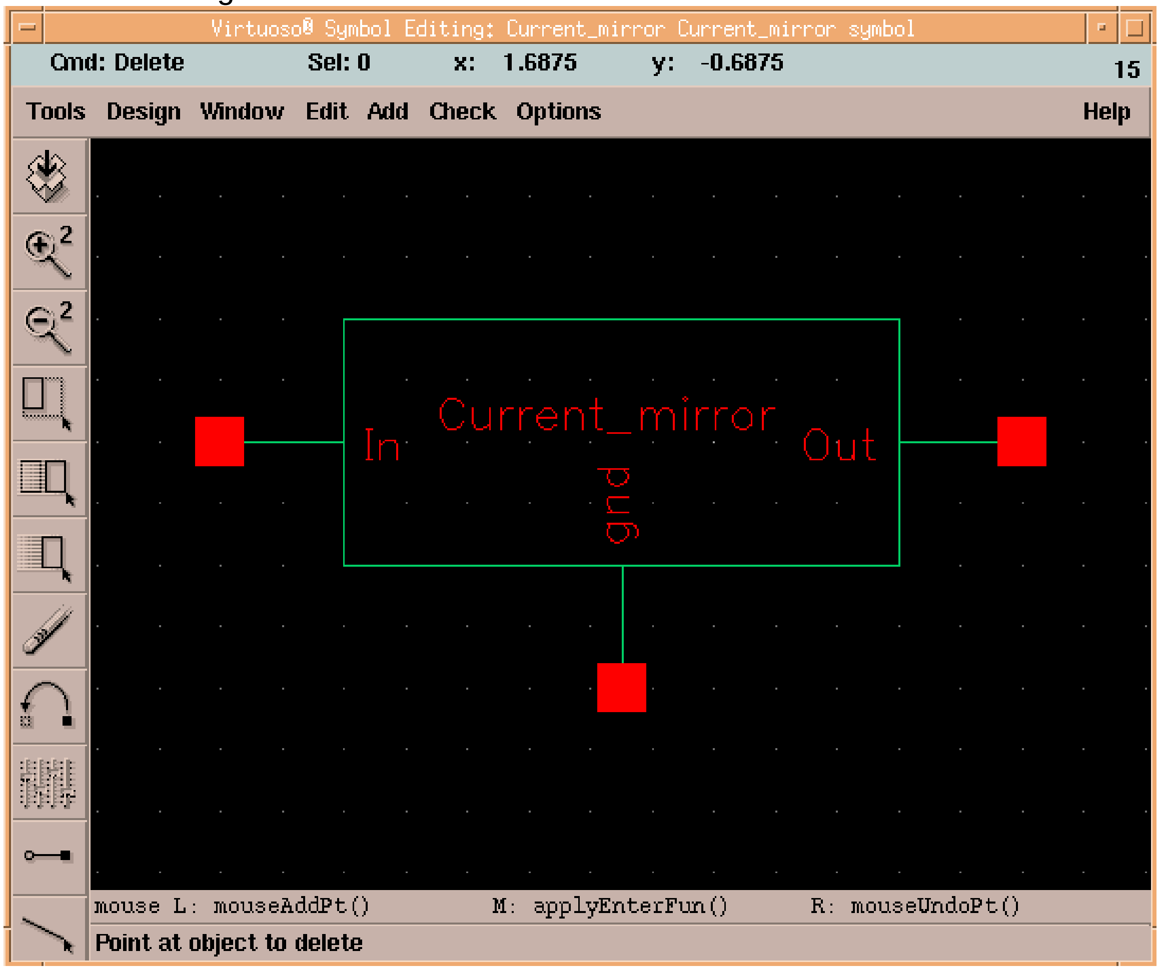
1. In the Virtuoso schematic window of the schematic you have created above, select **Design** → **Create Cellview** → **From CellView...** A **Cell View from** Cell View window appears, press **OK**.



2. In the **Symbol Generation Options** window you can define which Pins are Left, Right, Top or Bottom, then press **OK**.



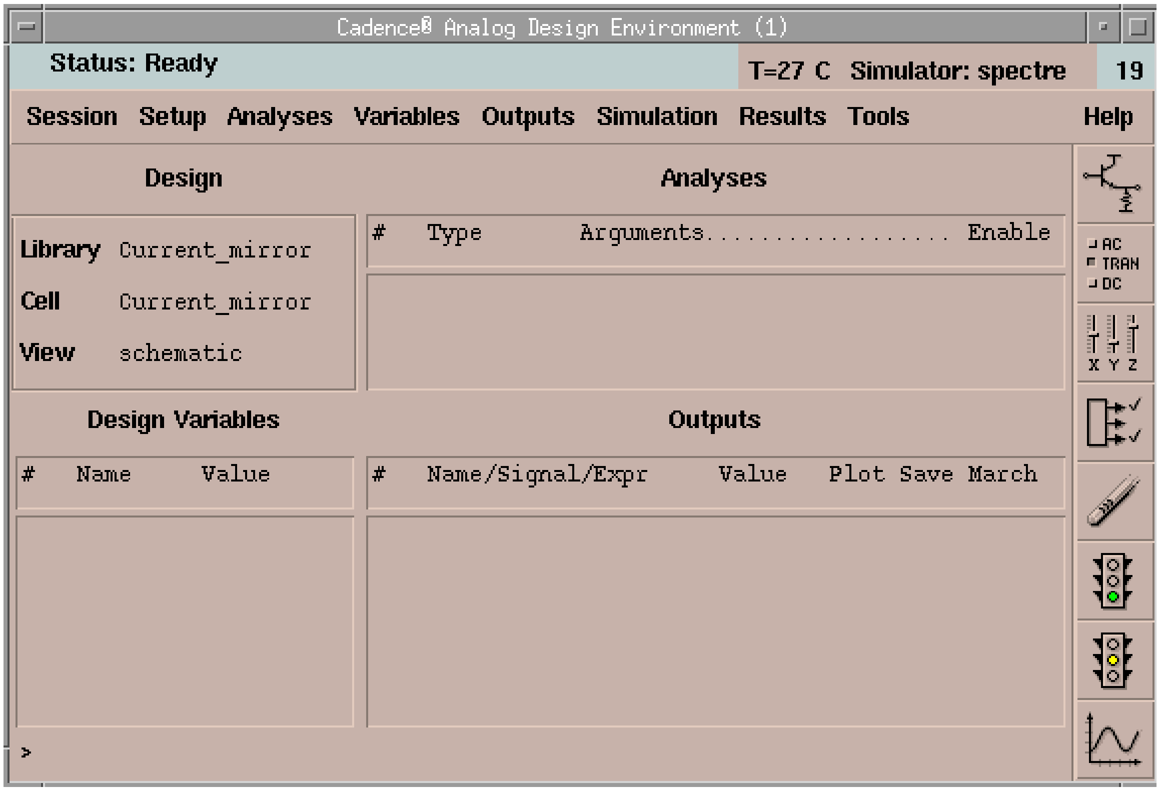
2. In the **Virtuoso Symbol Editing** window that appears, make modifications to make the symbol look as below. Replace [@partname] with the name Current_mirror. You may delete [@instanceName]. Save the symbol and exit using **Window** → **Close**.



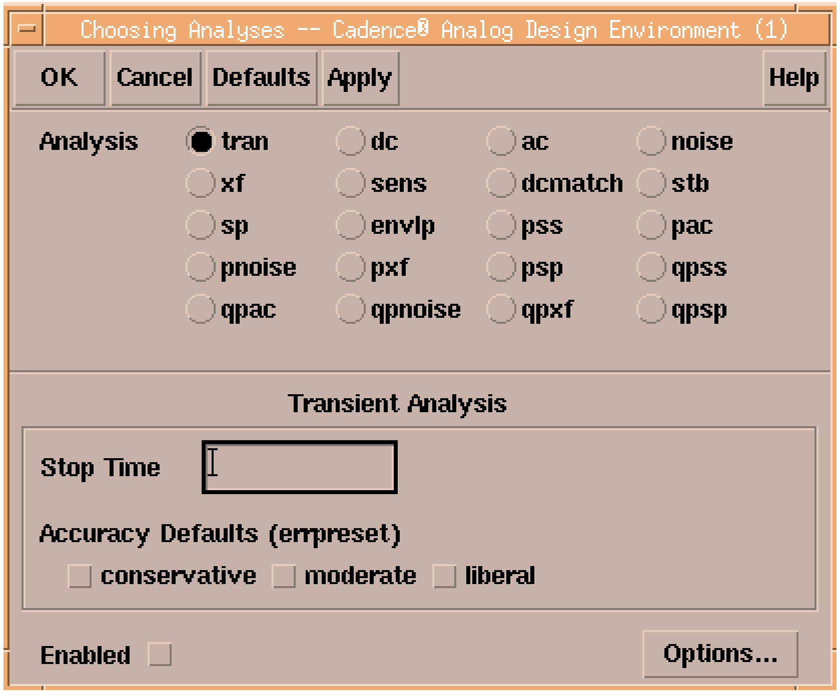
3. Now the Current_mirror is ready to be used in other schematics.

3 Analysis

In the Schematic Editor, select **Tools** → **Analog Environment**. In the **Cadence@ Analog Design Environment** Simulation Window that appears.



In the **Cadence@ Analog Design Environment** Window select **Analyses** a **Choosing Analyses** appear, there are many kinds of simulators and analysis methods. So all that you need to do in this window is to select the type of analysis you need and then select the nodes at which you want to observe the waveforms. You are encouraged to play around with the various menus and figure out how they make can your analysis easy and interesting.



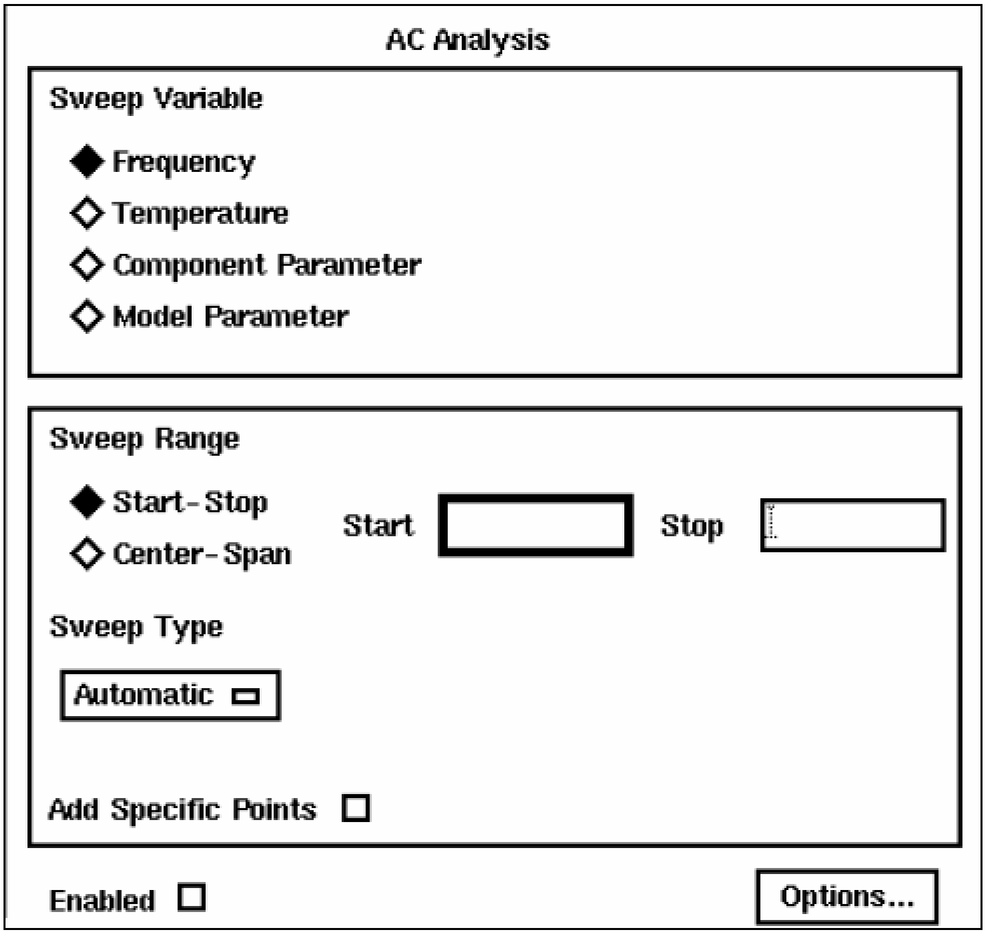
3.1 AC Small-Signal Analysis

AC small-signal analysis linearizes the circuit about the DC operating point and computes the response to a given small sinusoidal stimulus. Spectre can perform the analysis while sweeping a parameter.

The parameter can be a frequency, a design variable, temperature, a component instance parameter, or a component model parameter. If changing a parameter affects the DC operating point, the operating point is recomputed on each step.

To set up an AC small-signal analysis,

1. Choose **AC** from the Choosing Analyses form to display the appropriate options.



2. Choose a **sweep variable** option and specify any necessary parameters.

- If you do not sweep the frequency, specify the frequency at which to sweep the variable.
- If you sweep a design variable, fill out the name of the design variable, or select from the list box after hitting the select button.
- If you sweep a component, specify the parameter to sweep. Click Select Component to click in the Schematic window and select the component.
- If you sweep a model parameter, enter the model and parameter names.

3. Specify the **sweep range** and type.

Enter the start and stop points of the range or the center and span of the range.

The sweep type options are mapped to Spectre statements:

- Linear + Step Size = step
- Linear + Total Points = lin
- Logarithmic + Points Per Decade = dec
- Logarithmic + Total Points = log

- o Add Specific Points = values=[…]

4. Click Options to select the Spectre options controlling the simulation.

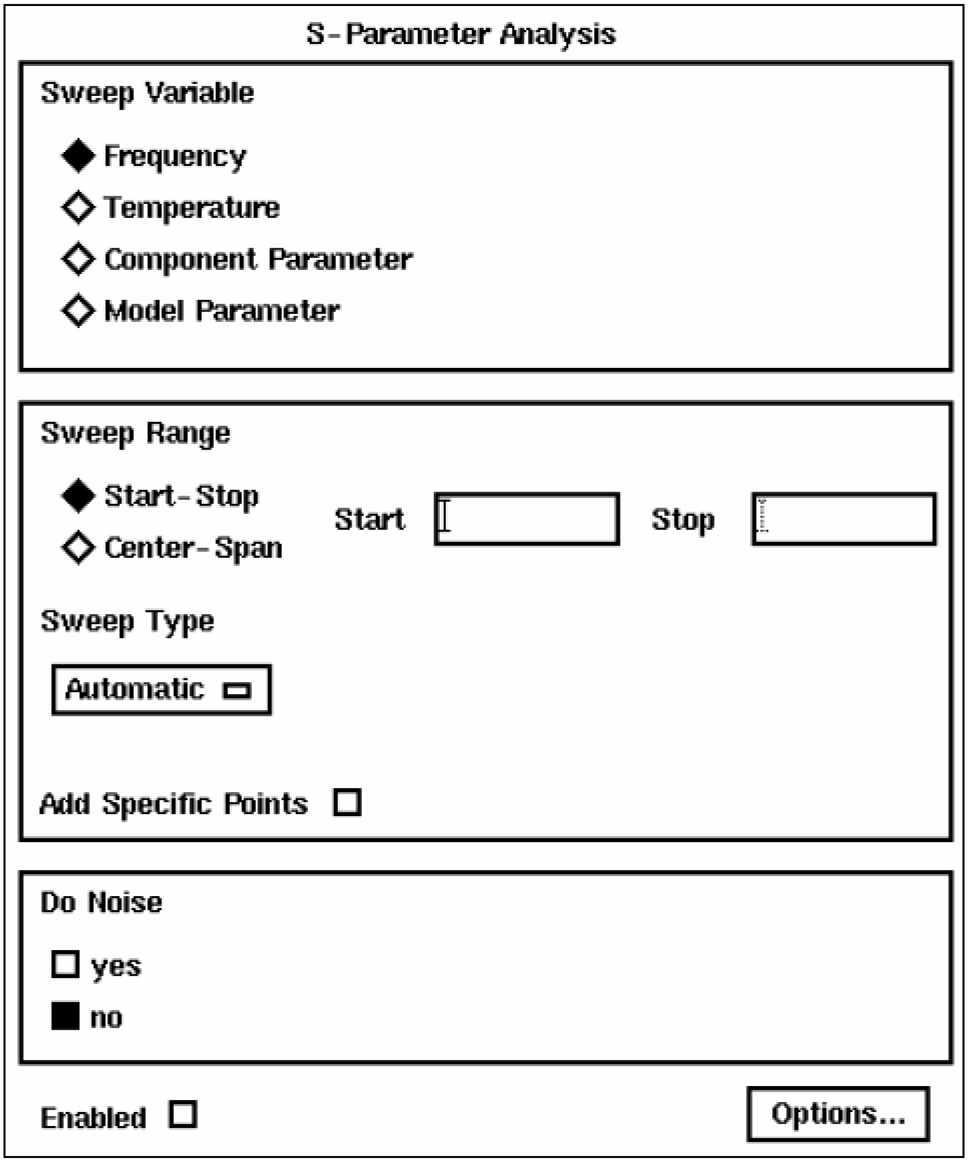
5. Click Enable and **Apply**.

3.2 S-Parameter Analysis

The S-parameter analysis linearizes the circuit about the DC operating point and computes S-parameters of the circuit taken as an N-port. The psin instances (netlist-to-Spectre port statements) define the ports of the circuit. Each active port is turned on sequentially, and a linear small-signal analysis is performed. The Spectre simulator converts the response of the circuit at each active port into S-parameters and prints these parameters. There must be at least one active port (analogLib psin instance) in the circuit.
The parameter can be a frequency, a design variable, temperature, a component instance parameter, or a component model parameter. If changing a parameter affects the DC operating point, the operating point is recomputed on each step.
To set up an S-parameter analysis,

1. Choose **sp** from the Choosing Analyses form to display the appropriate options.

2. Choose a **sweep variable** option and specify any necessary parameters.
- o If you do not sweep the frequency, specify the frequency at which to sweep the variable.
- o If you sweep a design variable, fill out the name of the design variable, or select from the list box after hitting the select button.
- o If you sweep a component, specify the parameter to sweep. Click Select Component to select the component in the Schematic window.
- o If you sweep a model parameter, enter the model and parameter names.



3. Specify the **sweep range** and type.

Enter the start and stop points of the range or the center and span of the range.

The sweep type options are mapped to Spectre statements:

- Linear + Step Size = step
- Linear + Total Points = lin
- Logarithmic + Points Per Decade = dec
- Logarithmic + Total Points = log
- Add Specific Points = values=[…]

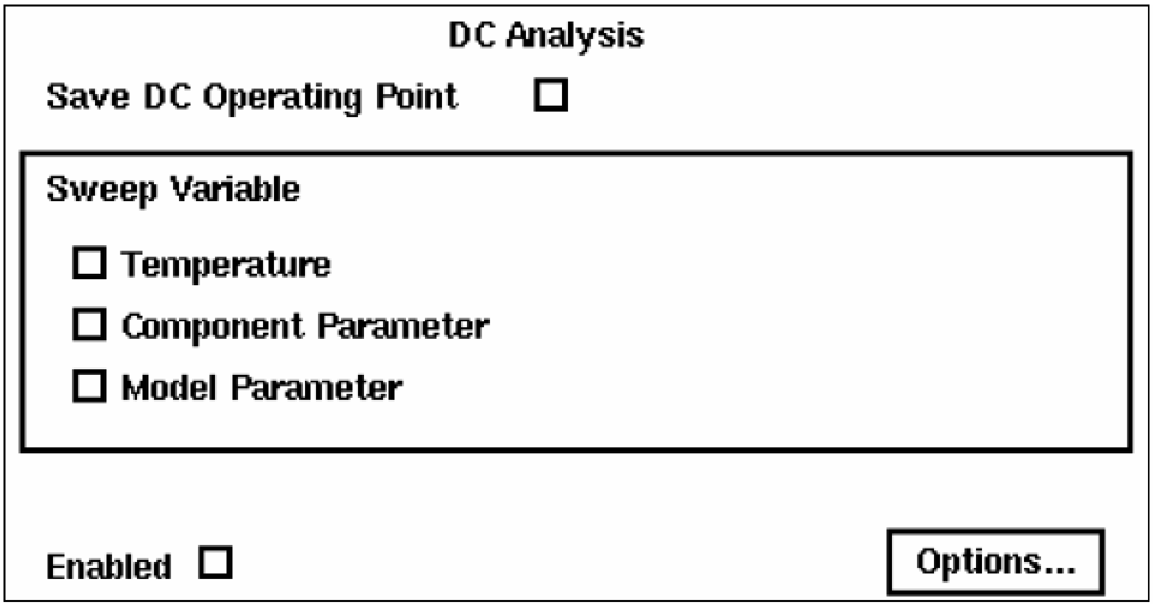
4. Click Options to select the Spectre options controlling the simulation.

5. Click the Noise radio button to perform noise analysis.

6. Click Enabled and **Apply**

3.3 DC Analysis

The DC analysis finds the DC operating point or DC transfer curves of the circuit. To generate transfer curves, specify a parameter and a sweep range. The parameter can be a temperature, a device instance parameter, or a device model parameter.



To save the DC operating point,

- ➢ Click Save DC Operating Point, click Enabled, and click Apply

Sweeping a Variable

To run a **DC** transfer curve analysis and sweep a variable,

1. Choose a sweep variable.
The Choosing Analyses form redisplays to show additional fields.

2. Specify the necessary parameters.

- o If you sweep a design variable, fill out the name of the design variable, or choose from the list box after pressing the select button.
- o To sweep a component, specify the component name and the parameter to sweep.
- o Use the select componentcommand to click in the Schematic window to select the component.
- o To sweep a model parameter, enter the model and parameter names.

3. Specify the sweep range and type.
The sweep type options are mapped to Spectre statements:

- o Linear + Step Size = step
- o Linear + Total Points = lin
- o Logarithmic + Points Per Decade = dec
- o Logarithmic + Total Points = log
- o Add Specific Points = values=[…]

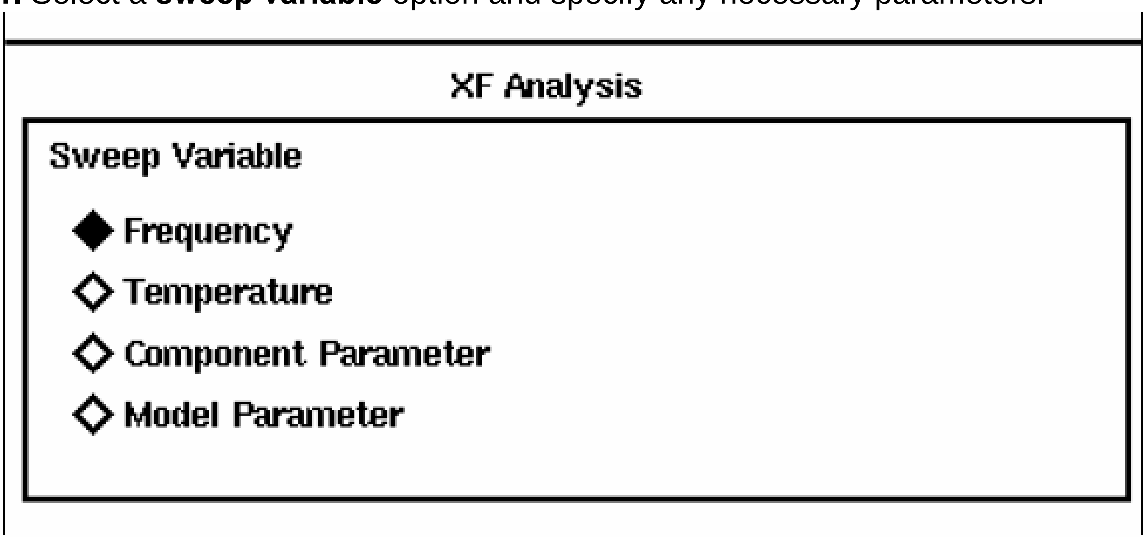
4. Click Options to set the spectreS options controlling DC simulation.

5. Click **Apply**.

3.4 Transfer Function Analysis

The transfer function, or xf, analysis linearizes the circuit about the DC operating point and performs a small-signal analysis that calculates the transfer function from **every independent source or instance terminal** in the circuit to a designated output. The variable of interest at the output can be voltage or current.

1. Select a **sweep variable** option and specify any necessary parameters.



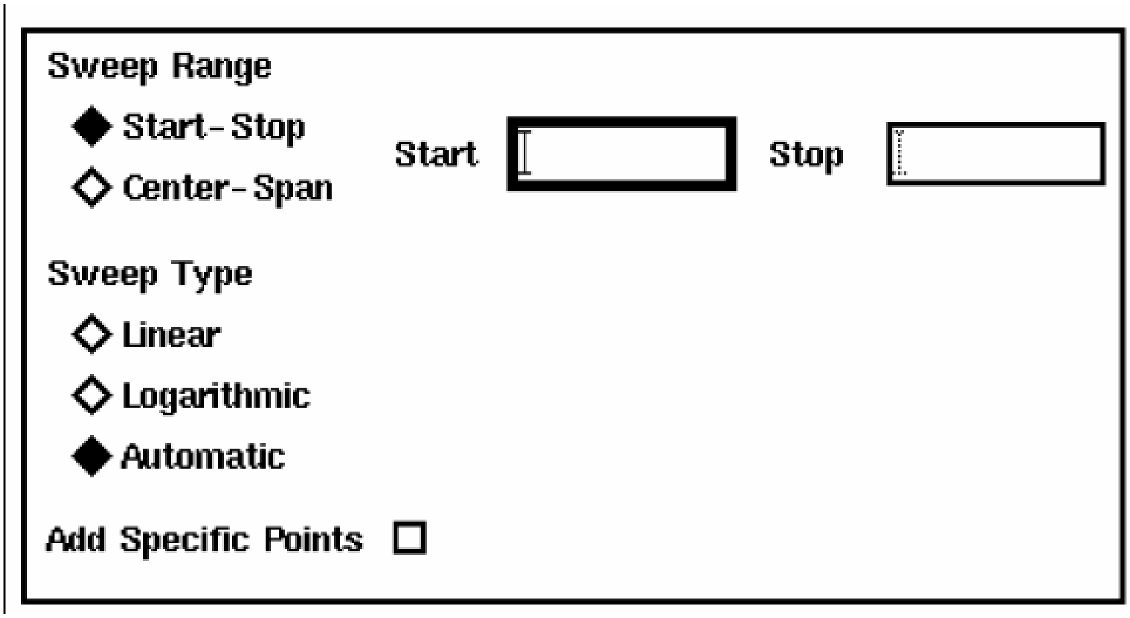
- o If you do not sweep the frequency, specify the frequency at which to sweep the variable.
- o If you sweep a design variable, fill out the name of the design variable, or select from the list box after hitting the select button.
- o If you sweep a component, specify the analysis frequency, component name, and the parameter to sweep. Use the select component command to click in the Schematic window to select the component.
- o If you sweep a model parameter, enter the model and parameter names.

2. Specify the **sweep range** and type.

The sweep type options are mapped to Spectre statements:

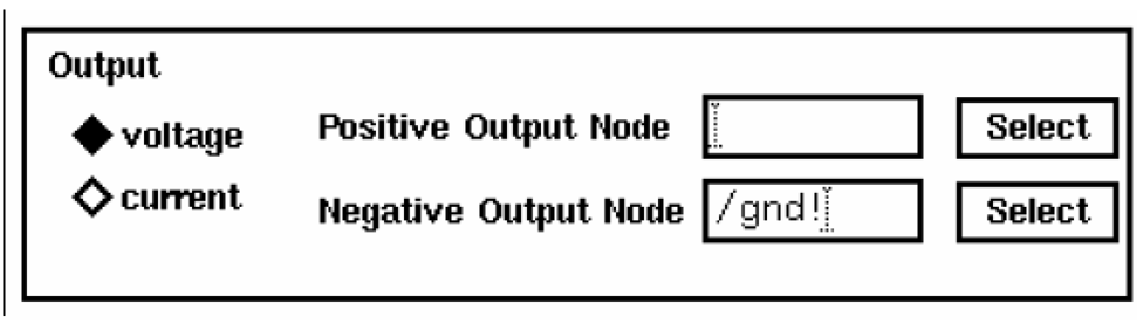
- o Linear + Step Size = step

- Linear + Total Points = lin
- Logarithmic + Points Per Decade = dec
- Logarithmic + Total Points = log
- Add Specific Points = values=[…]



3. Choose voltage or current for Output.

- To measure the output voltage, click Select opposite Positive Output Node and click a net in the schematic.
- To measure the output current, click current, click Select opposite Negative Output Node, and click an instance in the schematic.



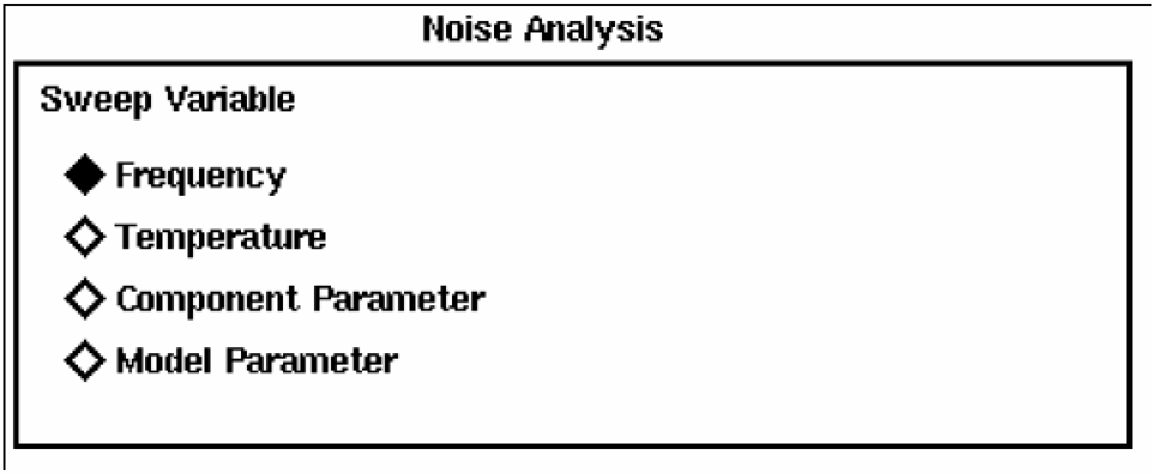
4. Click Options to set the spectreS options controlling transfer function simulation.

5. Click **Apply**.

3.5 Noise Analysis

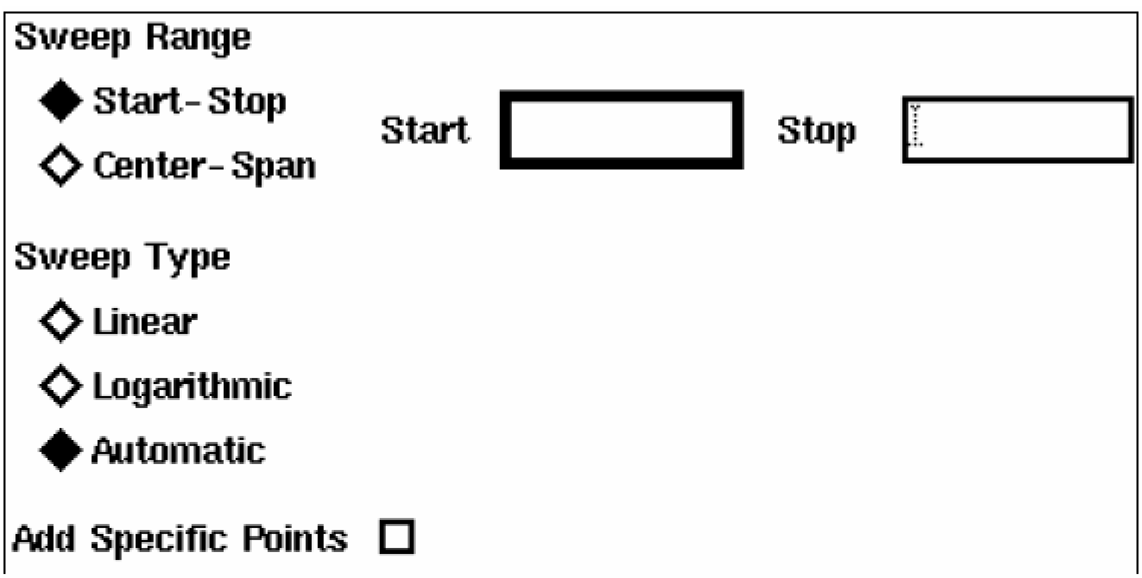
The noise analysis linearizes the circuit about the DC operating point and computes the totalnoise spectral density at the output. If you specify an input probe, the transfer function and the input-referred noise for an equivalent noise-free network is computed. To set up a noise analysis,

1. Choose a **sweep variable** option and specify any necessary parameters.



- If you do not sweep the frequency, specify the frequency at which to sweep the variable.
- If you sweep a design variable, fill out the name of the design variable, or choose from the list box after pressing the select button.
- If you sweep a component, specify the analysis frequency, component name, and the parameter to sweep. Use the select component command to click in the Schematic window to select the component.
- If you sweep a model parameter, enter the model and parameter names.

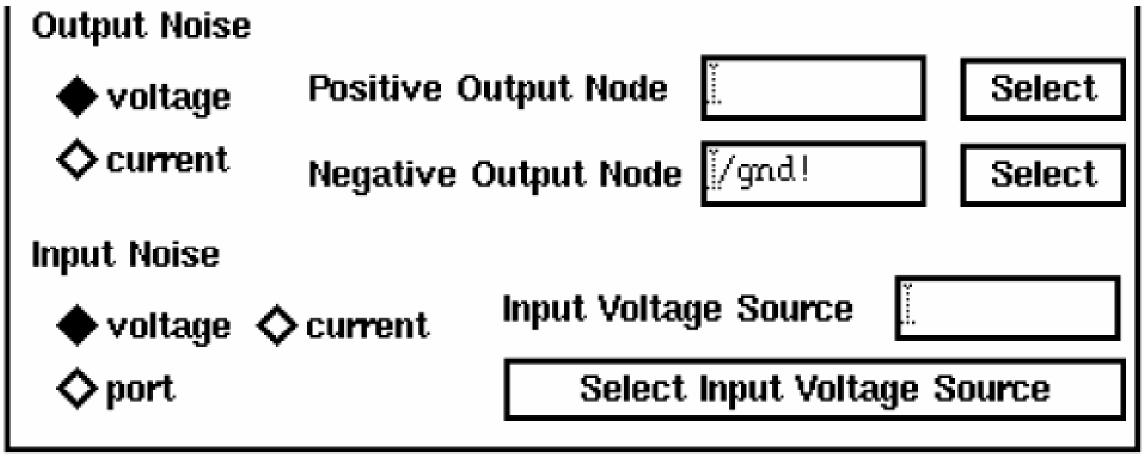
2. Specify the **sweep range** and type.



The sweep type options are mapped to Spectre statements:

- Linear + Step Size = step
- Linear + Total Points = lin
- Logarithmic + Points Per Decade = dec
- Logarithmic + Total Points = log
- Add Specific Points = values=[…]

3. Choose an **Output Noise option**.



- To measure the output noise voltage, click Select opposite Positive Output Node and click a net in the schematic.
- To measure the output noise current, click current, click Select opposite Negative Output Node, and click a voltage source in the schematic.

4. Optionally, **choose an Input Noise option**.

- Choose voltage, current, or port.
- Click Select Input.
- Click a source or port in the schematic.
- Click Apply.

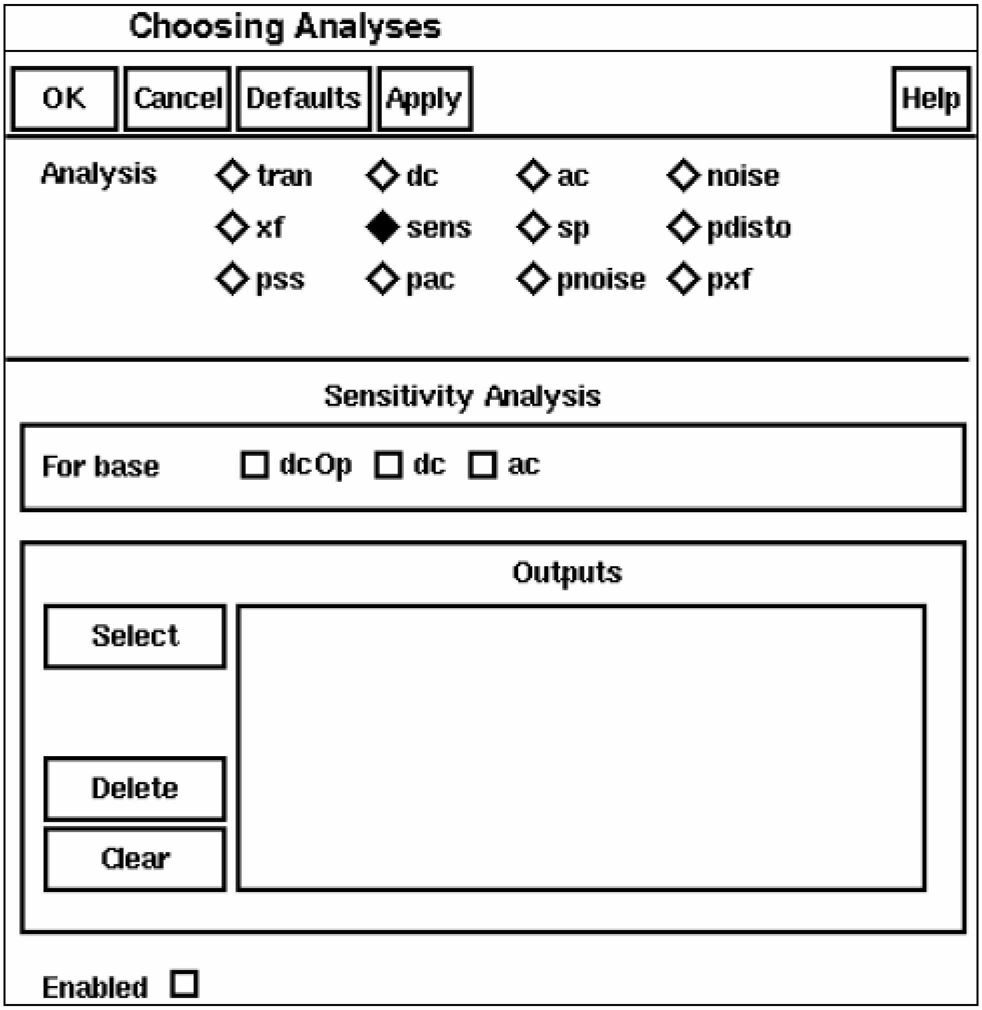
5. Click Options to set the spectreS options controlling noise simulation.

6. Click **Apply**.

3.6 Sensitivity Analysis

Sensitivity analysis lets a designer see which parameters in a circuit most affect the specified outputs. It is typically used to tune a design to increase or decrease certain design goals. You might run a sensitivity analysis to determine which parameters to optimize using the optimizer.

1. Choose the **sens** radio button on the Choosing Analyses form. The form redraws:



2. Choose which **types of sensitivities** you want to calculate.
In the **For base** field, choose any of the analyses on which you want to perform a sensitivity analysis. The available analyses are **dcOp**(DC operating point), **dc**, and **ac**.
Before you run a sensitivity analysis, you must run the corresponding base analysis.

3. Click **Select to select the outputs** you want to measure.
Select prompts you to select outputs by clicking on their instance in the schematic.
Outputs can be any nets or ports. When you click Select, the Schematic window moves to the front of the screen. The Schematic window must be open before you can select any outputs. Use the `Esc` key to end selection.

4. (Optional) In the Simulation window, choose Simulation – Options to open the Simulator Options form. Scroll down in the form to find the sensitivity options.

Type a filename in the sensfile field to specify a filename for the Spectre sensitivity results. This file is in ASCII format, and is generated in the psf directory. If you do not specify a value, the file is named sens.output by default.

5. View your results.

From the simulation window, choose Results – Print – Sensitivity. The results display in a print window.

Sensitivity Results - /hm/mdh/simulation/rlc/spectre/schematic/netlist/sens.output.sorted

File

AC sensitivity analysis for 'ac':

SweepParameter	SweepValue	OutputVariable	SensitivityReal	SensitivityImag	DesignParameter
freq	2.15443e+07	C9:1	-7.0443e+06	8.74235e+06	C8:c
freq	1e+07	C9:1	-6.2153e+06	3.585e+06	C8:c
freq	4.64159e+07	C9:1	-4.72496e+06	1.26848e+07	C8:c
freq	4.64159e+06	C9:1	-3.57924e+06	965817	C8:c
freq	1e+08	C9:1	-2.39979e+06	1.40469e+07	C8:c
freq	2.15443e+06	C9:1	-1.7526e+06	224163	C8:c
freq	1e+06	C9:1	-823336	51612.9	C8:c
freq	464159	C9:1	-383182	12928.5	C8:c
freq	215443	C9:1	-177964	4116.27	C8:c
freq	2.15443e+07	C9:1	707.095	576.534	C9:c
freq	1e+07	C9:1	621.236	1091.8	C9:c
freq	4.64159e+07	C9:1	477.417	180.964	C9:c
freq	4.64159e+06	C9:1	356.105	1352.21	C9:c
freq	1e+08	C9:1	245.679	43.4219	C9:c
freq	2.15443e+06	C9:1	172.957	1425.34	C9:c
freq	1e+06	C9:1	79.8075	1442.06	C9:c
freq	464159	C9:1	35.5014	1445.68	C9:c
freq	215443	C9:1	14.3965	1446.44	C9:c
freq	2.15443e+07	C9:1	0.000707095	0.000576534	C9:m
freq	2.15443e+07	C9:1	-0.00070443	0.000874235	C8:m
freq	1e+07	C9:1	-0.00062153	0.0003585	C8:m
freq	1e+07	C9:1	0.000621236	0.0010918	C9:m

3.7 Parametric Analysis

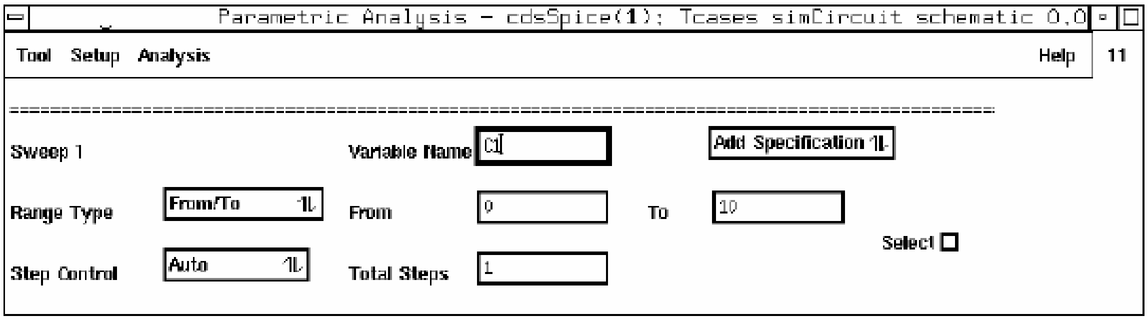
The parametric analysis feature (parametric plotting) lets you assign values to components and other parameters in a circuit and sweep the circuit over the ranges of specified values. You can display the results of the analysis as charts or different types of curves, depending on the values assigned to the axis and plotting parameters.

After running a parametric analysis, you can plot a group of curves for any waveform object in the netlist in a single display window. Each curve represents the results for a particular value in the sweep range, and you can compare the different curves to choose the best value.

From the **Affirma Analog Circuit Design Environment** Simulation Window, you can use the following procedure to call up the Parametric Analysis window:

- Choose **Tools** → **Parametric Analysis** in the Affirma analog circuit simulation window.

The Parametric Analysis window appears. You use this window to specify values for the parametric analysis. You can enter many specifications, and you can choose options from three main menus at the top of the window. These menus are Tool, Setup, and Analysis.



3.8 Corners Analysis

The corners tool provides a convenient way to measure circuit performance while simulating a circuit with sets of parameter values that represent the most extreme variations in a manufacturing process.
With the tool, you can compare the results for each set of parameter values with the range of acceptable values. By revising the circuit, if necessary, so that all the sets of parameters produce acceptable results, you can ensure the largest possible yield of circuits at the end of the manufacturing process.

To prepare for a corners analysis,

- Ensure that the design you use is simulatable with nominal design parameter values.
- Set up a simulation in the *Virtuoso® Analog Design Environment* window to run the analysis you want to use.
- Ensure that all design variables in the circuit have an initial value.
- In the Virtuoso Analog Design Environment window, choose **Tools → ADS → Cornertool…**

3.9 Other Analysis's

The SpectreRF analyses add several kinds of functionality to Spectre simulation.

- **Periodic Steady-State (PSS)** analysis
- **Periodic Small-Signal analyses**
  - **Periodic AC (PAC) analysis**
  - **Periodic S-Parameter (PSP) analysis**
  - **Periodic Transfer Function (PXF) analysis**
  - **Periodic Noise (Pnoise) analysis**
- Periodic Distortion (Pdisto) analysis
- Quasi-Periodic Noise (QPnoise) analysis
- **Envelope Following analysis**

Periodic Steady-State (PSS) analysis is a large-signal analysis that directly computes the periodic steady-state response of a circuit. With PSS, simulation times are independent of the time constants of the circuit, so PSS can quickly compute the steady-state response of circuits with long time constants, such as high-Q filters and oscillators. You can perform sweeps using PSS; you can sweep frequency, a time period, or a variable.
After completing a PSS analysis, the SpectreRF simulator can model frequency conversion effects by performing one or more Periodic Small-Signal analyses (PAC, PSP, PXF, and Pnoise). The periodic small-signal analyses, Periodic AC analysis (PAC), Periodic SParameter analysis (PSP), Periodic Transfer Function analysis (PXF) and Periodic Noise analysis (Pnoise), are similar to the Spectre AC, SP, XF, and Noise analyses, but you can apply them to periodically driven circuits that exhibit frequency conversion. Examples of important frequency conversion effects include conversion gain in mixers, noise in oscillators, and filtering using switched-capacitors.
Therefore, with Periodic Small-Signal analyses you apply a small signal at a frequency that may not be harmonically related (noncommensurate) to the periodic response of the undriven system, the clock. This small signal is assumed to be small enough so that it is not distorted by the circuit.

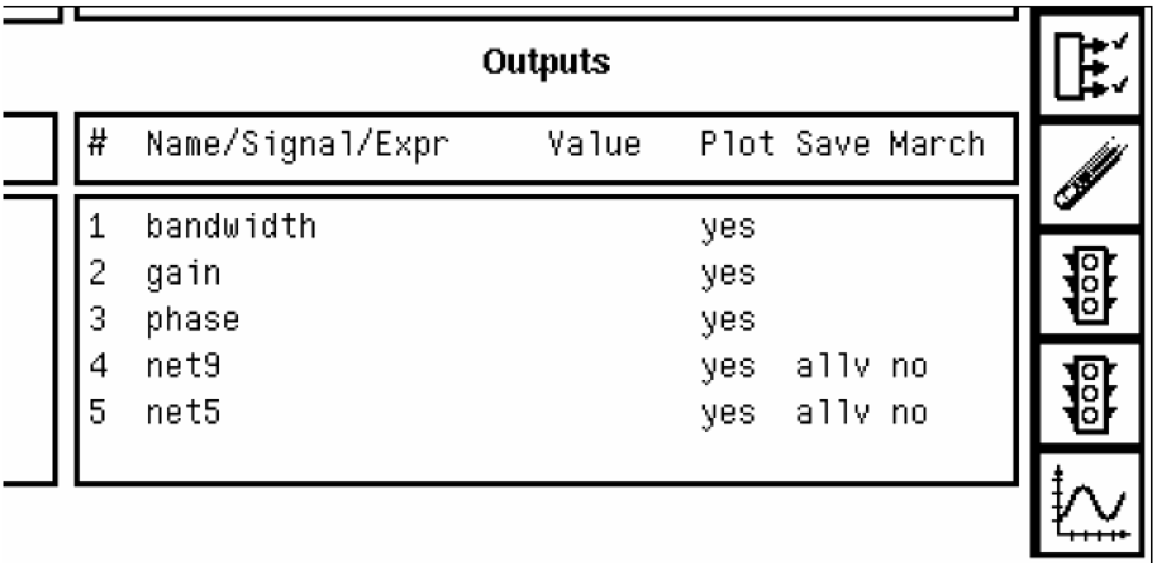
Periodic Distortion (Pdisto) analysis, a large-signal analysis, is used for circuits with multiple large tones. With Pdisto, you can model periodic distortion and include harmonic effects.
(Periodic small-signal analyses assume the small signal you specify generates no harmonics). Pdisto computes both a large signal, the periodic steady-state response of the circuit, and also the distortion effects of a specified number of moderate signals, including the distortion effects of the number of harmonics that you choose.
With Pdisto, you can apply one or two additional signals at frequencies not harmonically related to the large signal, and these signals can be large enough to create distortion. This analysis is also called Quasi-Periodic Steady-State analysis.

4 About the Saved, Plotted, and Marched Sets of Outputs

The Affirma analog circuit design environment keeps track of three sets of nets and terminals:

- The saved set, for which simulation data is written to disk
- The plotted set, which is automatically plotted after simulation in the Waveform window the plotted set can also contain expressions.
- The marched set, which is plotted in the Marching Waveform window during simulation

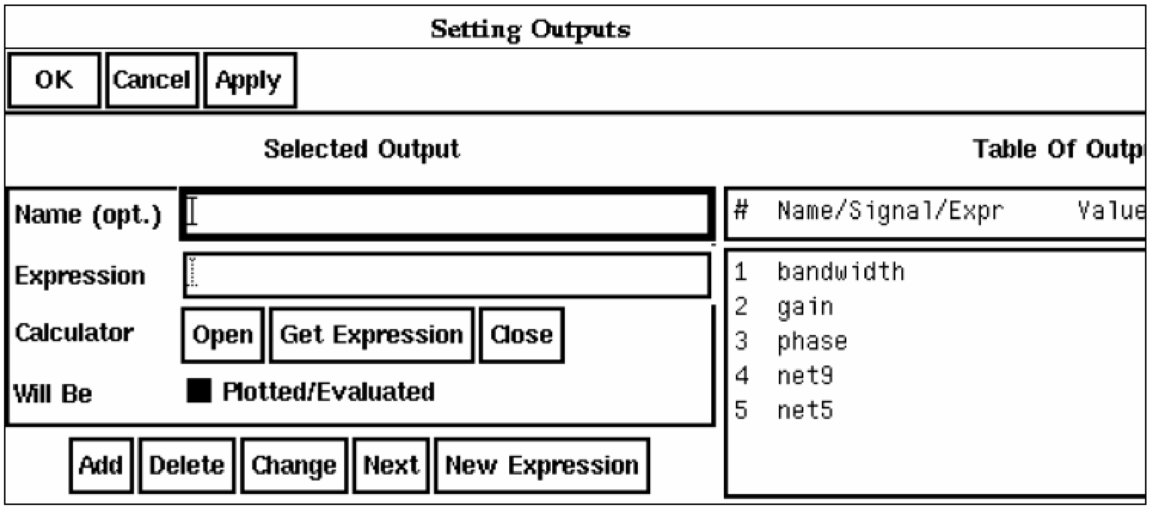
In the figure below, all five signals will be plotted and two will be saved after simulation. None will be marched during simulation.



Opening the Setting Outputs Form

You set up the saved, plotted, and marched sets of outputs with the Setting Outputs form.

- ➢ In the Simulation window, choose **Outputs** → **Setup**, or from the Schematic window, choose **Setup** → **Outputs**.



Saving All Voltages or Currents

To save all of the node voltages and terminal currents,

1. In the Simulation window, choose **Outputs** → **Save All**, or in the Schematic window, choose **Setup** → **Save All.**

2. Select the values you want to save and click **OK**.

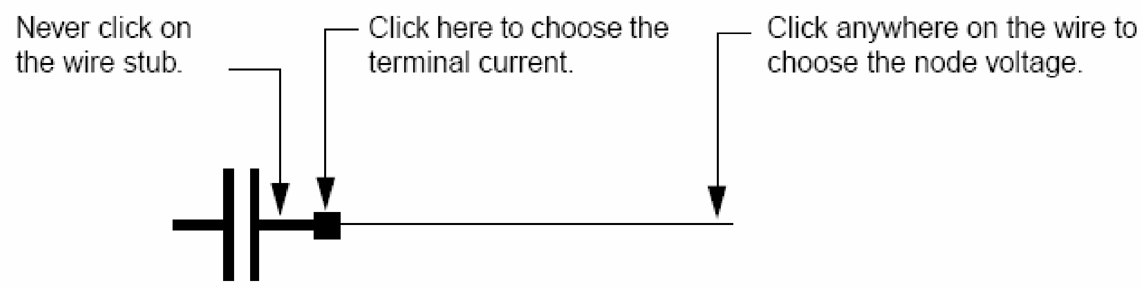
Note: When you set up a noise analysis with cdsSpice only, the system turns these options off. If you later deactivate the noise analysis, the system reactivates the Select all options.

Saving Selected Voltages or Currents

To save the simulation data for particular nodes and terminals,

1. In the Simulation window, choose **Outputs** → **To Be Saved** → **Select on Schematic**, or in the Schematic window, choose **Setup** → **Select on Schematic** → **Outputs to be Saved**.

2. In the Schematic window, **choose one or more nodes or terminals**. The system circles pins when you choose a current and highlights wires when you choose a net.
   - Click on an instance to choose all instance terminals.
   - Click on the square pin symbols to choose currents.
   - Click on wires to choose voltages.
   - Click and drag to choose voltages by area.



3. Press the Esc key when you finish.

Removing Nodes and Terminals from a Set
To remove a node or terminal from the saved, plotted, or marched set,

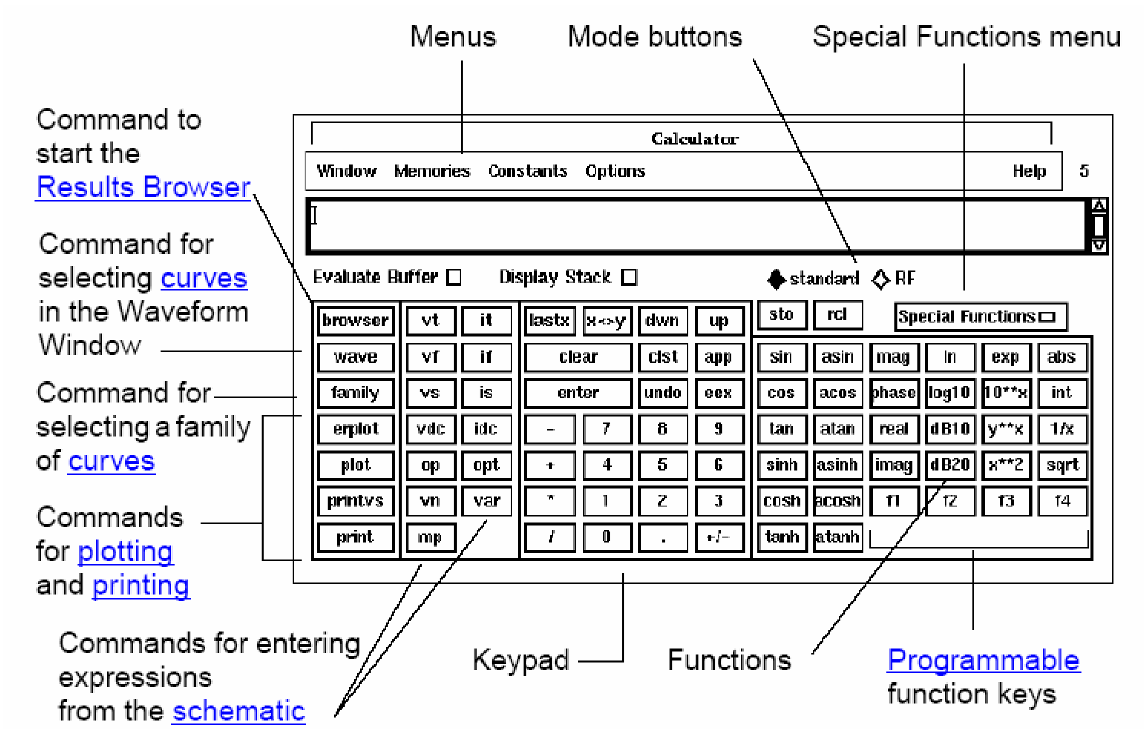
3. In the Simulation window, choose **Outputs** → **Setup**, or in the Schematic window, choose **Setup** → **Outputs**.
4. Double-click on the node or terminal in the Table Of Outputs list box.
5. Click to deselect the appropriate Will Be boxes.
6. Click Change.

Note: To remove a node from all three sets (delete it), highlight the node in the Simulation window and choose Outputs – Delete.

Showing DC Properties
Except node voltages, DC currents, transconductance (gm) etc. are also of concern. To see these parameters, from the **Affirma Analog Circuit Design Environment** Simulation Window choose **Results** → **Print** → **DC Operating Points**, and then **click** on the **Instance** in the **Virtuoso Schematic Editing** window. A new window shows the DC properties will pop up.

5 About the Calculator

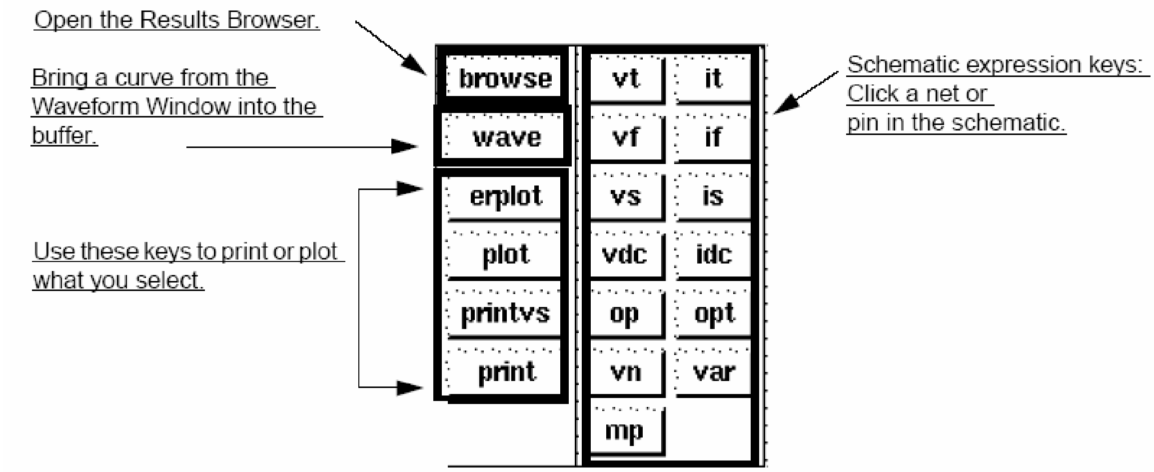
In the **Affirma Analog Circuit Design Environment** Simulation Window choose **Tool → Calculator.** The calculator has several kinds of buttons.



Selecting Data

There are three ways to bring simulation results into the calculator. You can

- Use the schematic expression keys to click nets and pins in the schematic and select their results
- Use the Results Browser to select results out of the UNIX file system hierarchy
- Use the *wave* command to select a curve in the Waveform Window



Selecting Data in a Schematic Window

The schematic expression keys let you enter data into the calculator buffer by selecting objects in the Schematic window.

Note: To use the *vn*, *var*, *op*, *opt*, or *mp* functions, you must either select results or have just run a simulation.

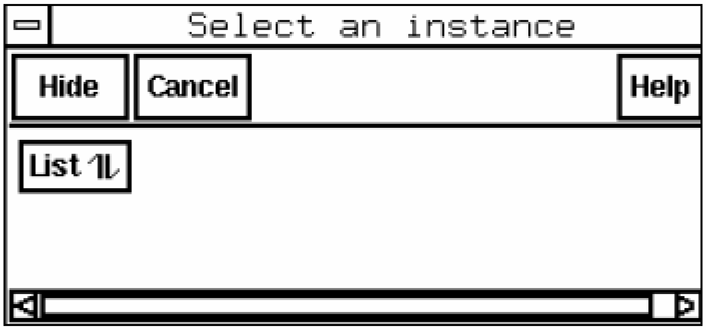
vt transient voltage	***it*** transient current
vf frequency voltage	***if*** frequency current
vs source sweep voltage	***is*** source sweep current (I vs V curves)
vdc DC voltage	***op*** DC operating point
vn noise voltage	***opt*** transient operating point
var design variable	***mp*** model parameter

1. Click a schematic expression key.
2. Click the appropriate object in the schematic.
   If more than one parameter is available for the expression and instance you picked, a form appears. Select the parameter you want from the List field and click OK.
3. When you have finished selecting objects, press the Esc key while the cursor is in the Schematic window.

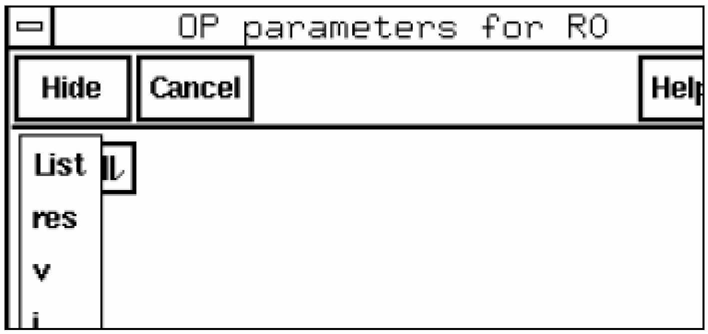
Choosing Parameters from Schematic Data

To select a parameter in the schematic with a schematic expression key

1. Click an instance in the schematic.



2. Choose the parameter you want from the List field.



Note: When you use the *op*, *opt*, *mp*, *vn*, or *var* functions, you must have just run a simulation, or you must choose *select results* from the *Results* menu in the Simulation window. Otherwise, the system does not know what to display.

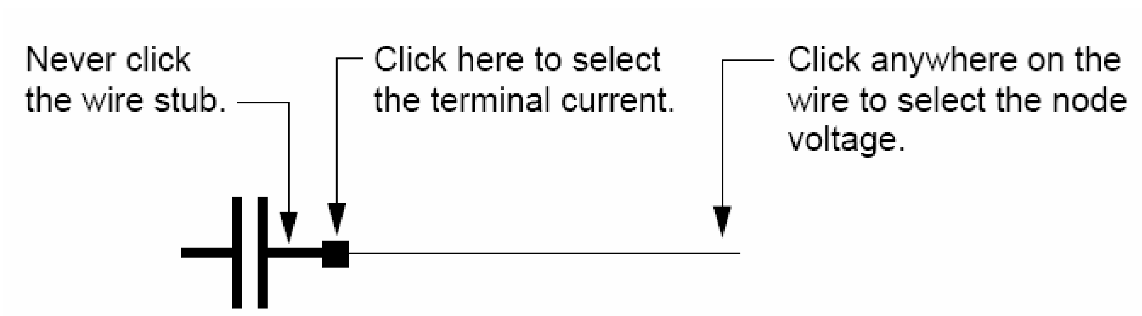
Choosing Voltages or Currents

To select voltages in the schematic

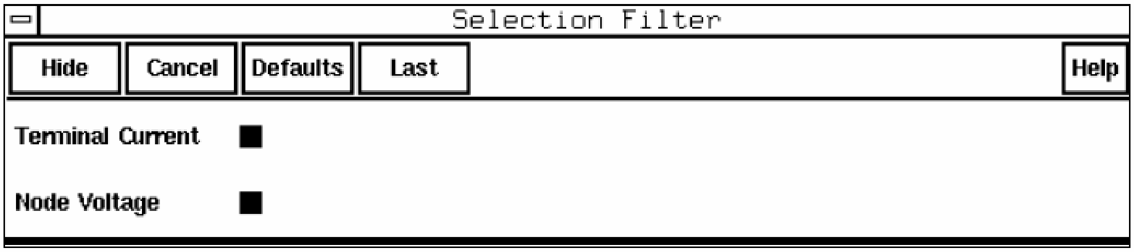
- Click wires.

To select currents

- Click square pin symbols, not wires.



You can use the Selection Filter form to restrict selection to either pins or wires. Press *F3* if the Selection Filter form did not appear.



Selecting Curves in the Waveform Window

Use the wave key to create an expression from a curve in the Waveform Window and place the expression into the calculator buffer.

1. Click *wave* in the calculator.
2. Click a curve in a Waveform Window.
The waveform expression that the system enters in the calculator is the expression on the Waveform Window status banner at the tracking cursor location.

Plotting or Printing Results

You can plot or print the value of the calculator buffer expression against an independent variable.
You can plot or print only the expressions that are in the buffer, not the memories. You must recall memory expressions into the buffer to plot or print them.

Plotting Expressions

To erase the Waveform Window and plot the buffer expression

- Click ***erplot*** in the calculator.

To plot the buffer expression without first erasing the Waveform Window

- Click ***plot*** in the calculator.

For example, to plot the I vs. V curve after a DC source-sweep analysis

1. In the calculator, click *IS*.
2. In the schematic, click the output terminal of the device.
Terminals are the square symbols at the end of the wire stub.
Now you have an expression in the buffer for the IV curve.
3. Click *erplot* in the calculator.

The system opens a Waveform Window (unless one is already open) and draws the curve.

Single-Expression Functions

These functions operate on only a single expression in the buffer.

Key	Function	Key	Function
mag	magnitude	*exp*	e^x
phase	phase	*10**x*	10^x
real	real component	*y**x*	y^x
imag	imaginary component	*x**2*	x^2
ln	base-e (natural) logarithm	*abs*	|x| (absolute value)
log10	base-10 logarithm	*int*	integer value
dB10	dB magnitude for a power expression	*1/x*	inverse
dB20	dB magnitude for a voltage or current	*sqrt*	$\sqrt{x}$

Example: Plotting the Magnitude of a Signal

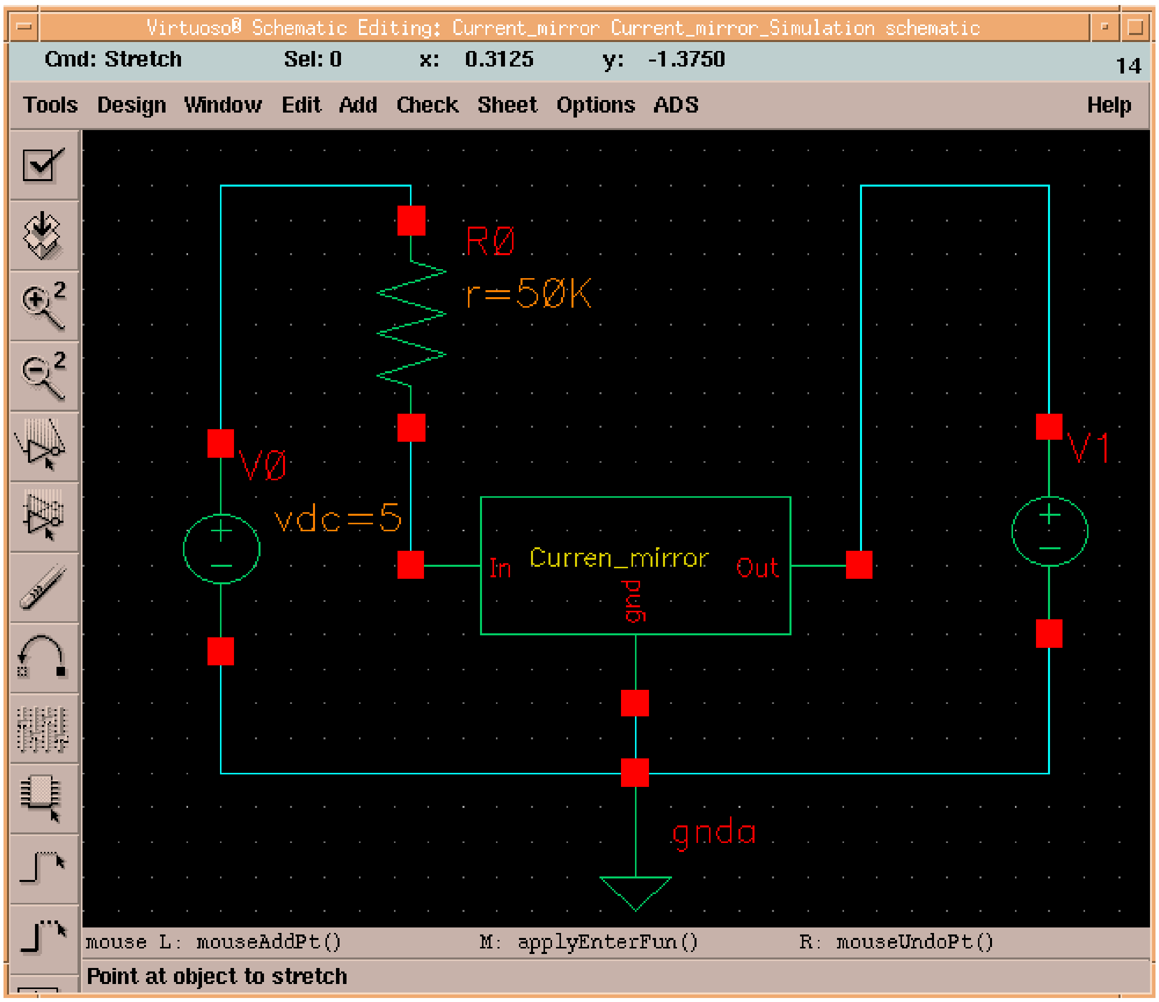
To plot the dB magnitude of a signal after an AC analysis

1. Click *vf* on the calculator.
2. On the schematic, click the net you want to plot.
3. With the cursor in the Schematic window, press the Esc key.
This cancels the *vf* function. Otherwise, the command stays active.
4. Click *dB20* on the calculator.
The calculator buffer now contains the expression you want to plot.
5. Click *plot* to show the curve.

6 Examples

6.1 Simple Current mirror Simulation

Create a new cell “Current_mirror_Simulation”. The schematic is shown below:

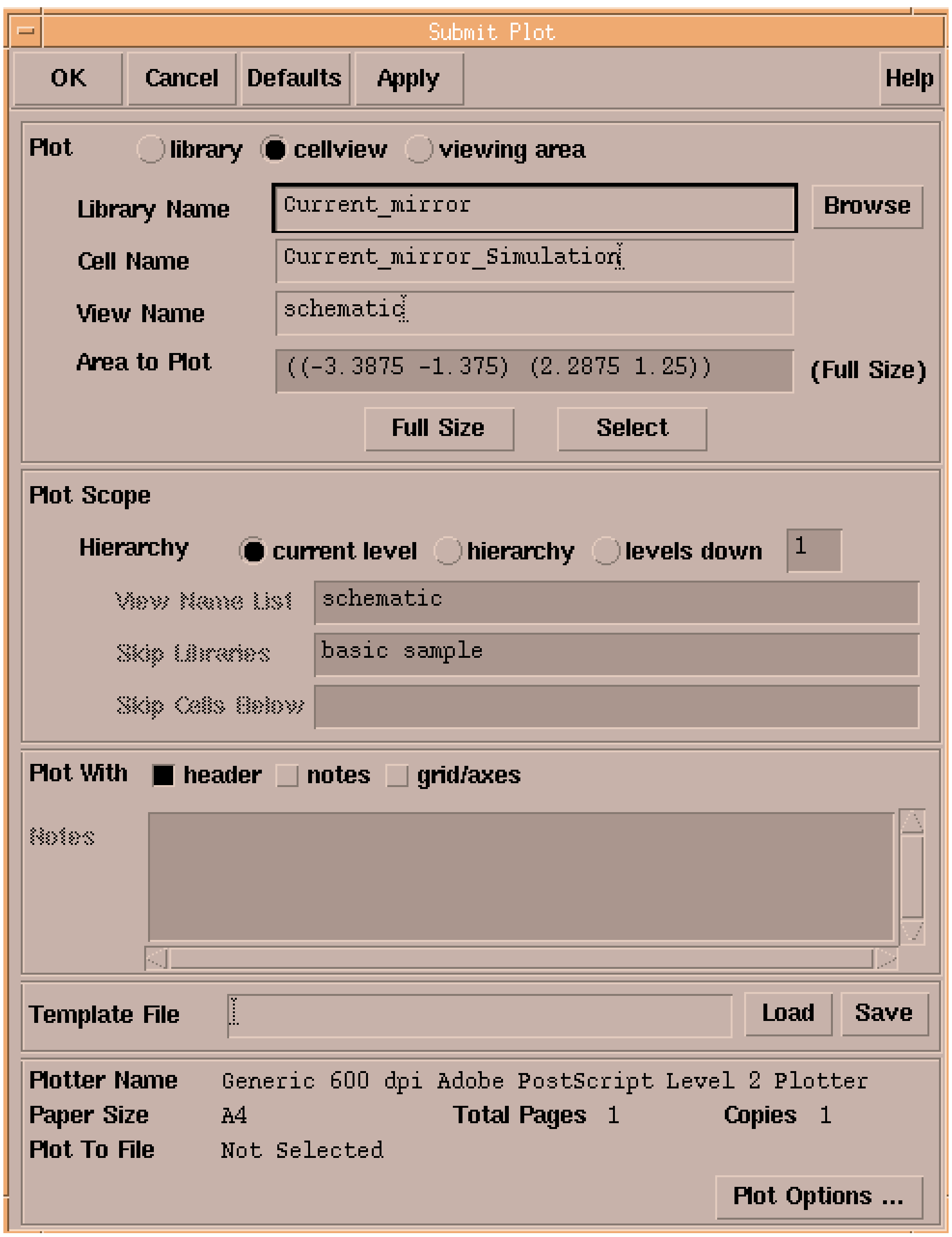


Insert the following instances “**I**”:
Current_mirror symbol what we have done before
res from the AnalogLib Library
vdc from the AnalogLib Library
gnda from the AnalogLib Library
connect the instances with wire “**W**” then press **Check & Save**.

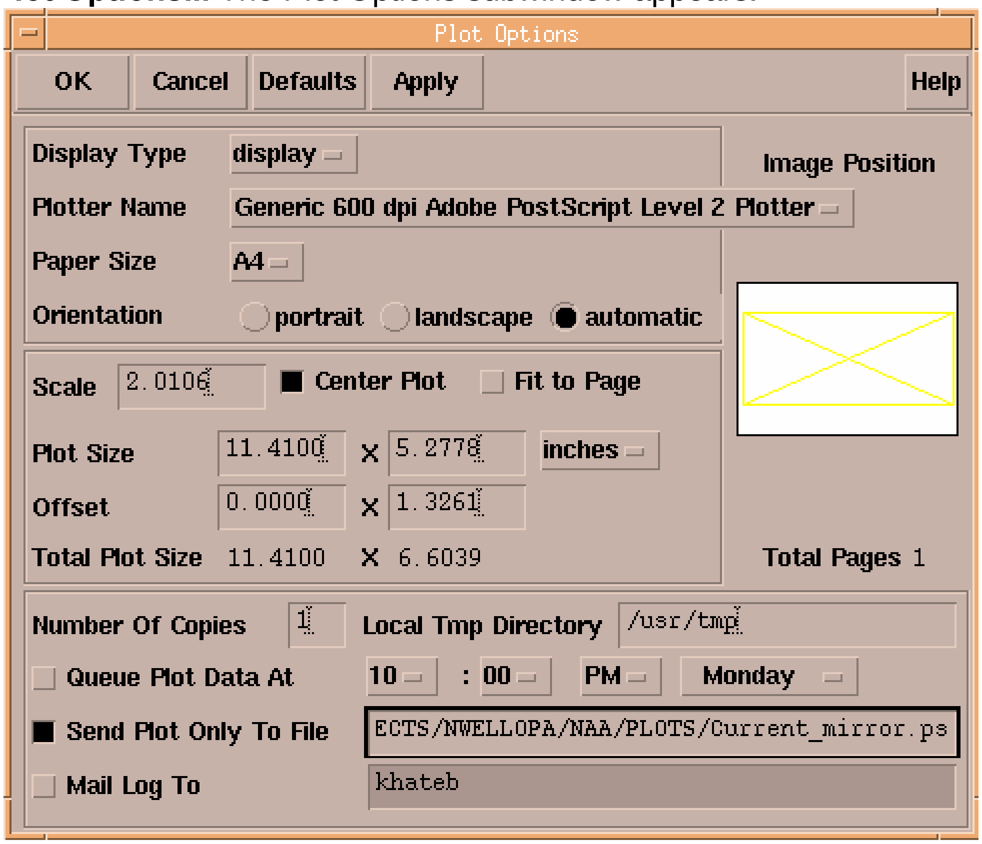
> **Notice:**
> The most used libraries are:
> **AnalogLib** for instances used for simulation purpose such: resistor, capacitor, voltage and current supply,…
> **TransistorLib** for instances related to the used technology as: transistors, resistors (type: hipo, nwell, Rdummy, poly,..), capacitors (typ: Cdummy, cpp,..)

Printing your Schematic

Now that the schematic is complete, you could print it out. To do this, in the **Virtuoso Schematic Editing** window, choose **Design** → **Plot** → **Submit**... The **submit plot** window appear.



Click **Plot Options...** The Plot Options subwindow appears.



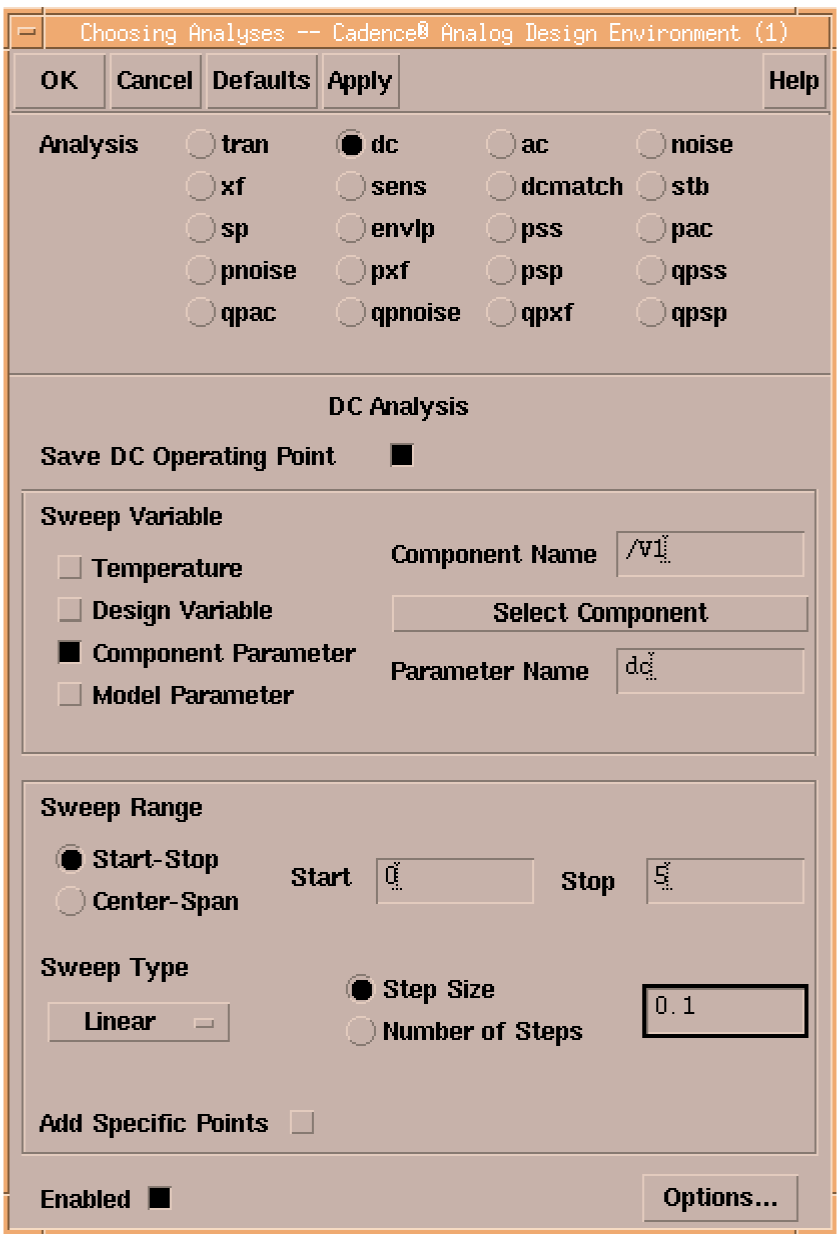
Check the "**Send Plot Only To File**" and type in a descriptive name about the plot. Be sure to end the name with the "**.ps**" or "**.eps**" extension, as seen above. What you are plotting is a postscript file. When the machine is done creating the file, it will send you mail telling you that it completed successfully. To prevent this, you can uncheck "**Mail Log To**".
Press **Ok** at **Plot Options** window and then press **OK** at **submit plot** window. Now the plot of your schematic is done.

Simulator Setup

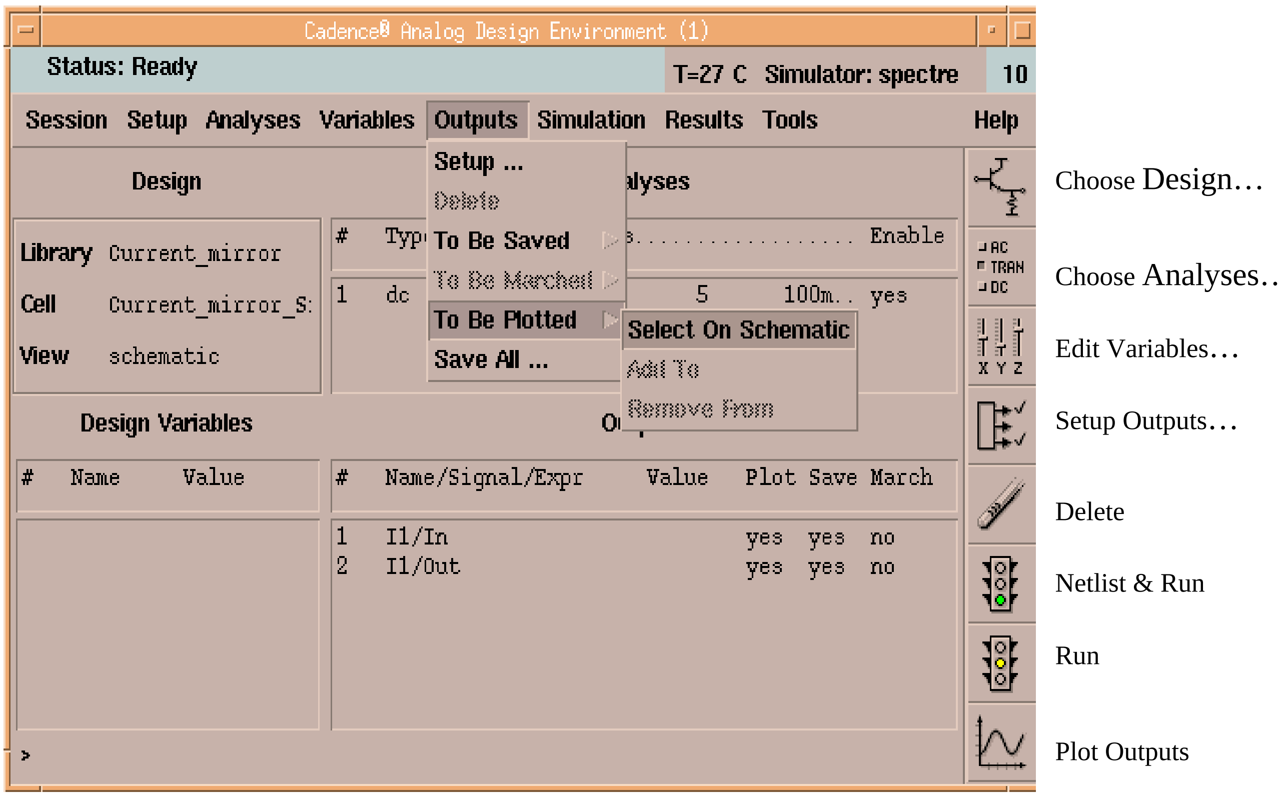
In **Virtuoso Schematic Editing** window, choose **Tools** → **Analog Environment** to start the simulation tool **Analog Design Environment**

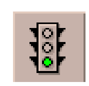
DC Simulation

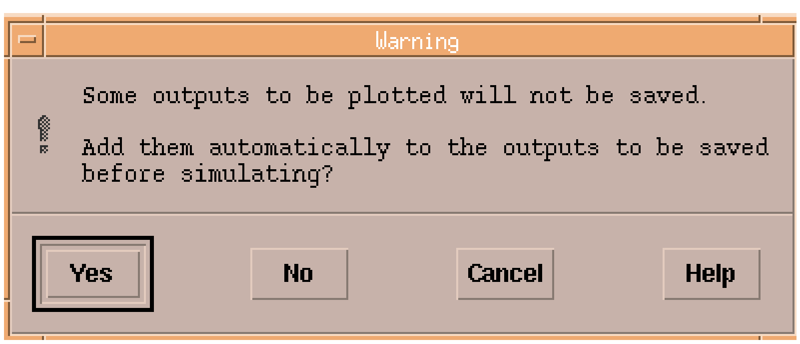
In the **Analog Design Environment** window, choose **Analyses** → **Choose,** In the pop-up window, click on **dc** analysis and choose to **Save DC Operating Point**, select the **Component Parameter** then click on **Select Component** then you can choose the component you want to sweep directly from the schematic, in our case the dc parameter of **V1**, then click **OK**.

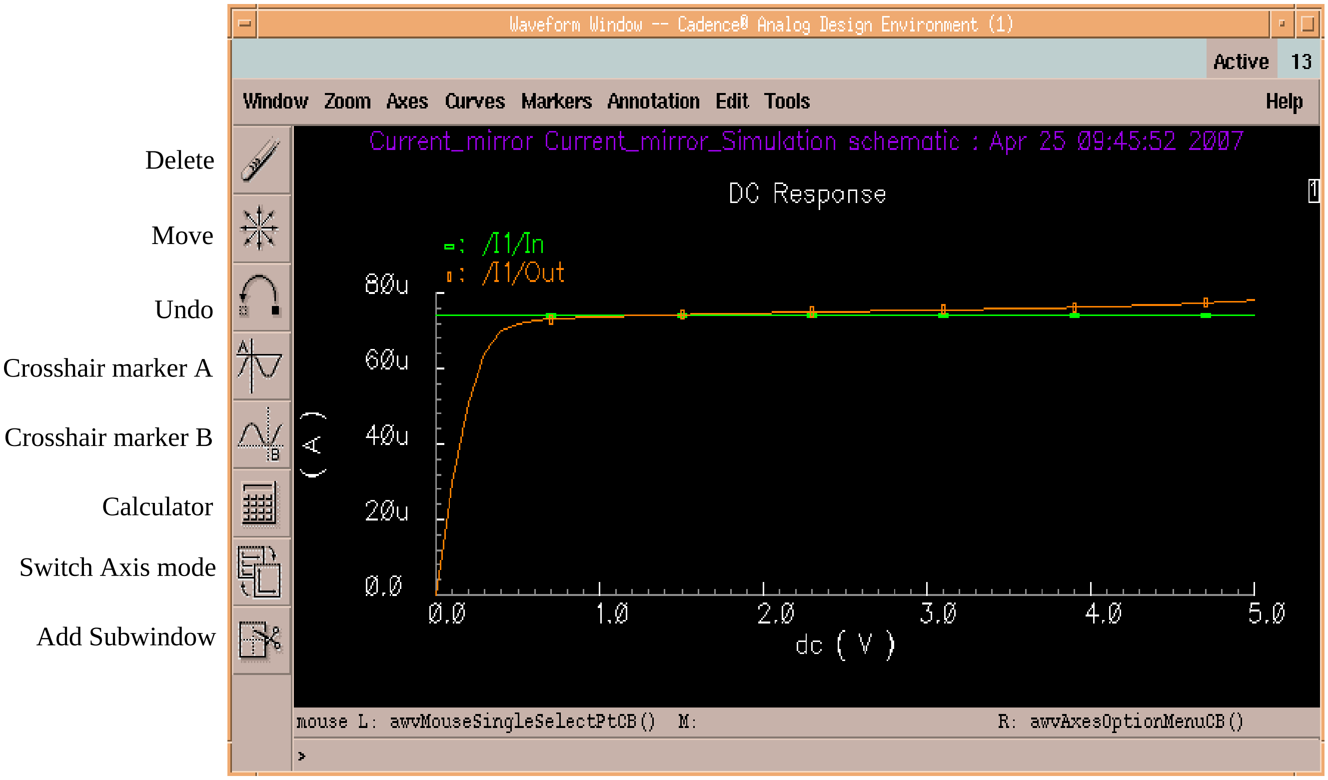


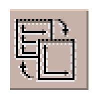
In the **Analog Design Environment** window, choose **Outputs → To Be Plotted → Select On Schematic**. In the **Schematic Editing** window click on the terminals **In** and **Out** of the **Current mirror**, then click **Esc**. In the **Outputs** of the **Cadence Analog Design Environment** on appears **I1/In** and **I1/Out**.



Now you can run the simulation: **Simulation → Netlist and Run** or press  a **Warning message** to save the outputs before simulating, click **Yes**.



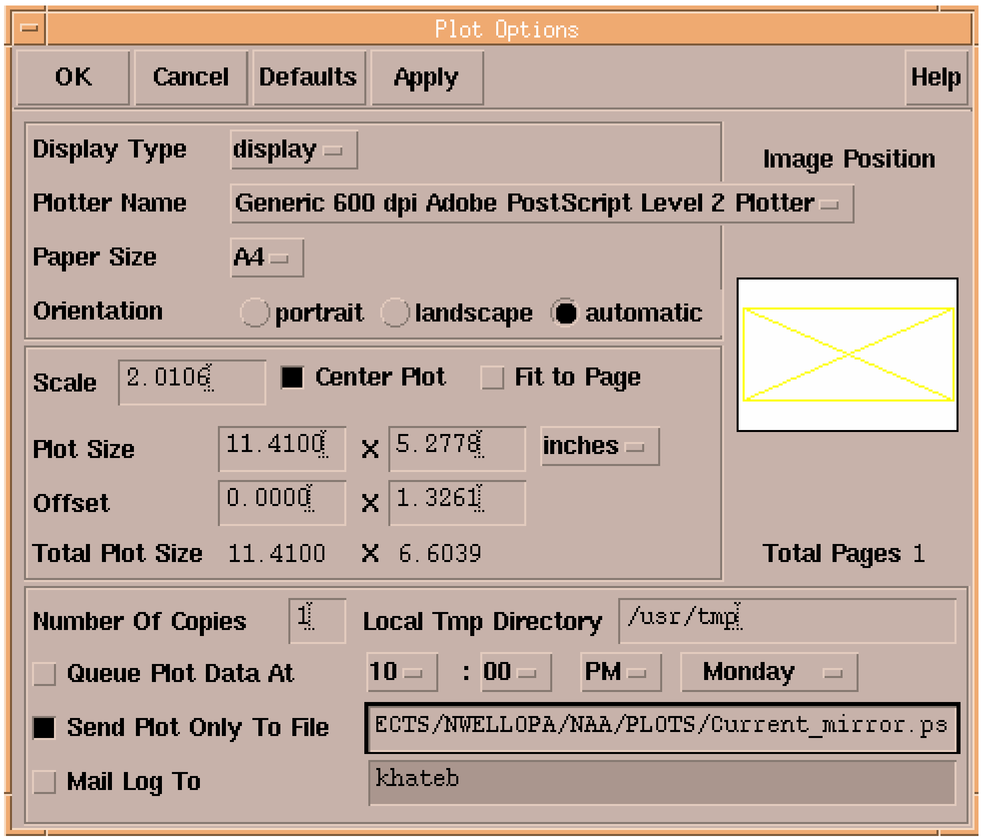


You can split the wave form by pressing **Switch Axis mode** 

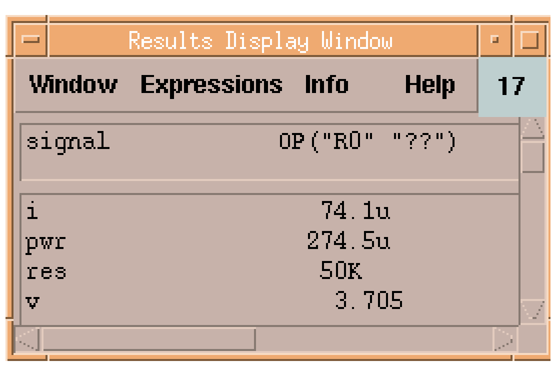
To display **Grid** to **Waveform Window,** press **Axes** → **Options…** and check **Grid** then press **OK**.

To read some value on the **Waveform Window** choose **Croohair marker A** eventually **B**.

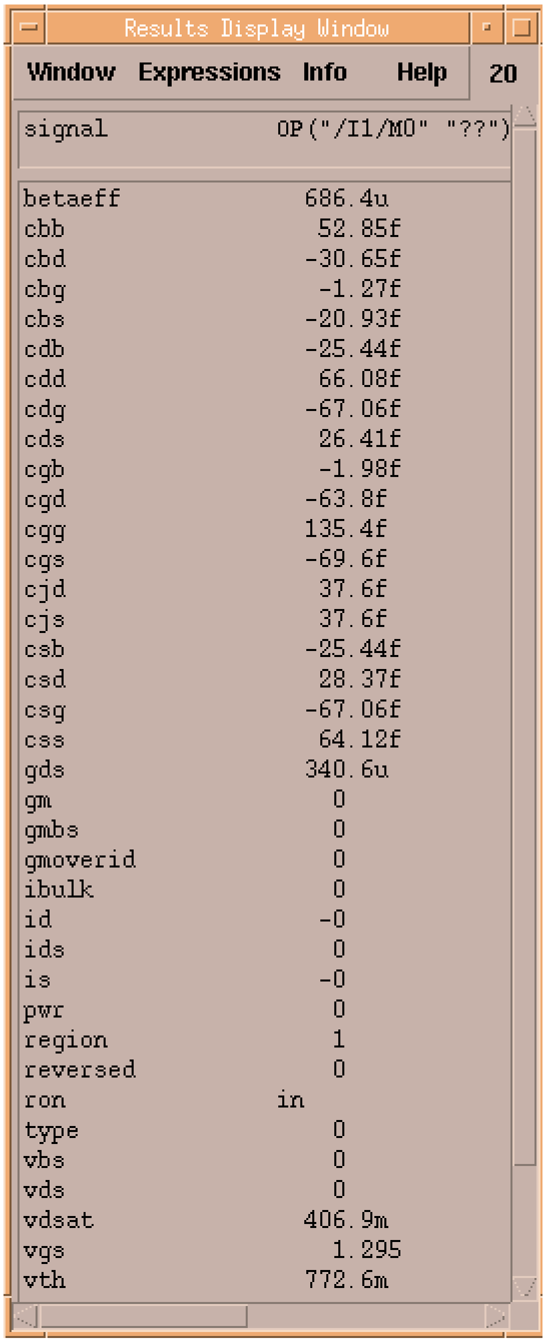
Printing out your waveform:
At **Waveform Window** press **Windows → Hardcopy …,** enable **Send Plot Only To File**, and type in a descriptive name about the plot. Be sure to end the name with the "**.ps**" or "**.eps**" extension. Later you can see the plot with ps browser tools.



DC operating points:
Except node voltages, DC currents, transconductance (gm) etc. are also of concern. To see these parameters, from the **Analog Design Environment** window, choose **Results → Print → DC Operating Points**, and then click on the instance in the "Schematic Editing" window. A new window as below will pop up.



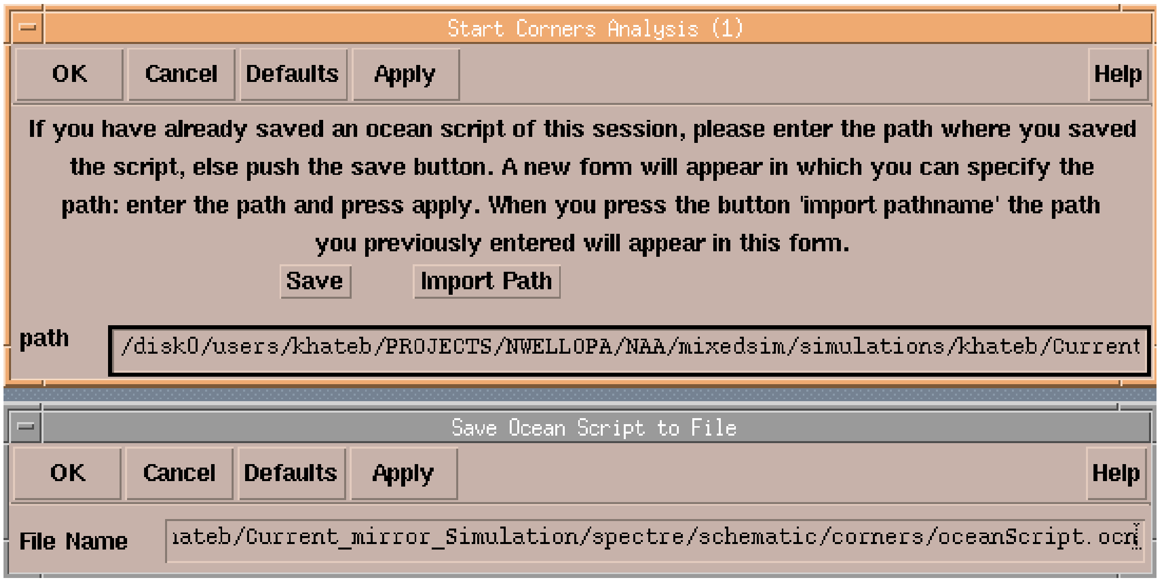
To see the DC operating point of the M_NMOS transistor of the current_mirror symbol, first click on it and then press “**V**” Now you choose in the same way: **Results** → **Print** → **DC Operating Points**, and then click on the instance in the “Schematic Editing” window. A new window as below will pop up



signal	OP("/I1/M0" "??")
betaeff	686.4u
cbb	52.85f
cbd	-30.65f
cbg	-1.27f
cbs	-20.93f
cdb	-25.44f
cdd	66.08f
cdg	-67.06f
cds	26.41f
cgb	-1.98f
cgd	-63.8f
cgg	135.4f
cgs	-69.6f
cjd	37.6f
cjs	37.6f
csb	-25.44f
csd	28.37f
csg	-67.06f
css	64.12f
gds	340.6u
gm	0
gmbs	0
gmoverid	0
ibulk	0
id	-0
ids	0
is	-0
pwr	0
region	1
reversed	0
ron	in
type	0
vbs	0
vds	0
vdsat	406.9m
vgs	1.295
vth	772.6m

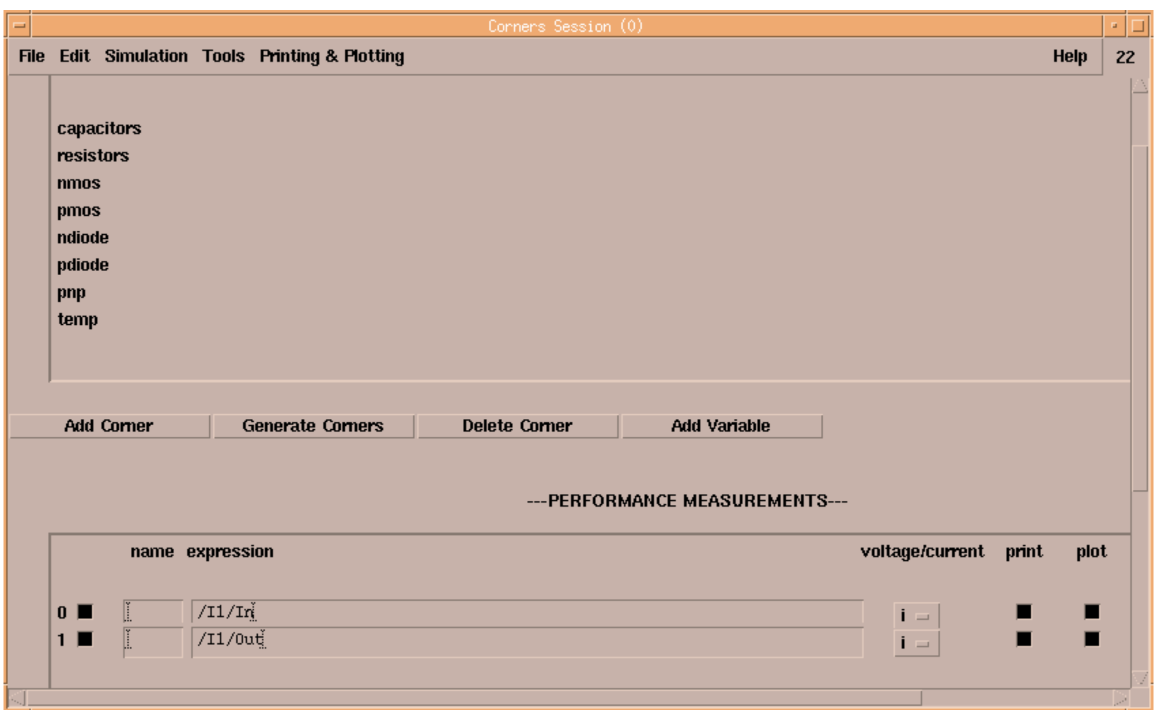
Corners Analyses:

In the Virtuoso Analog Design Environment window, choose **Tools** → **ADS** → **Cornertool…**, **Start Corner Analysis** window appears, click **Save** and chooce the **File Name** where you want to save the corner analyses result (usally copy

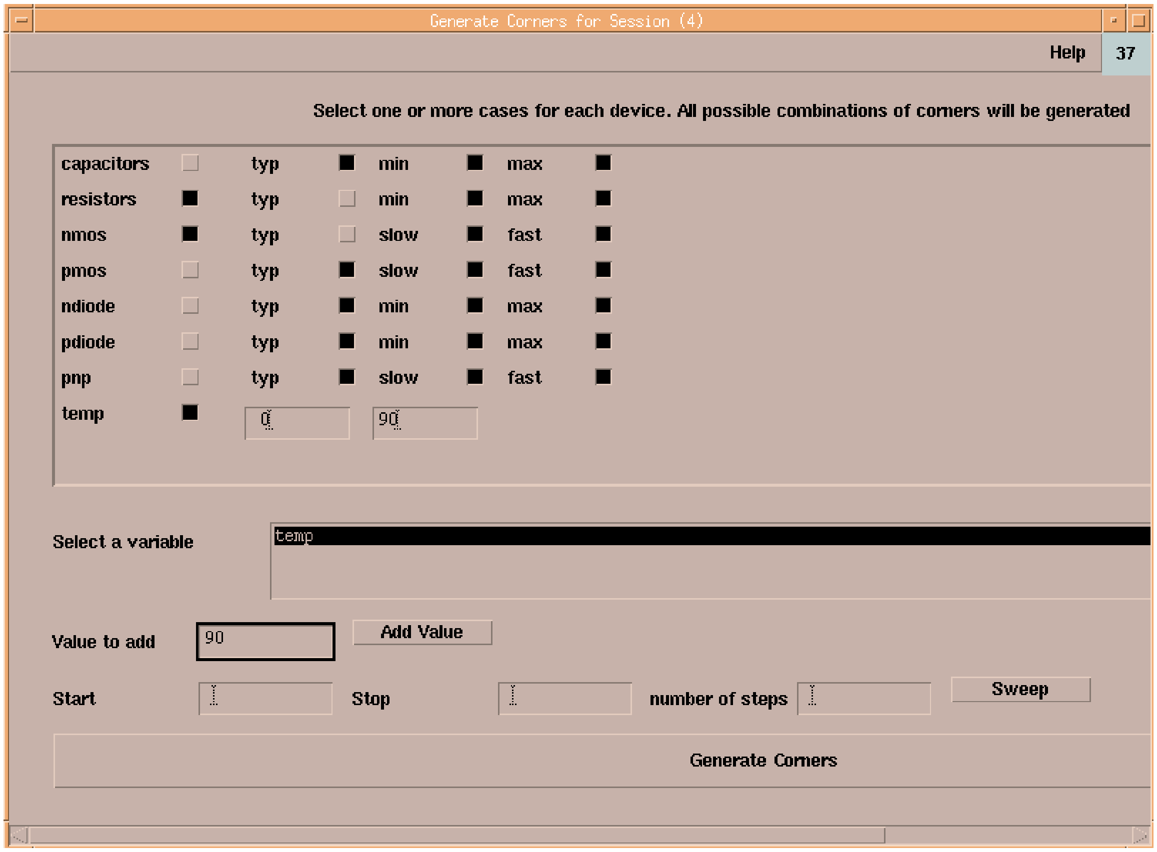


the path and paste it on the File Name).

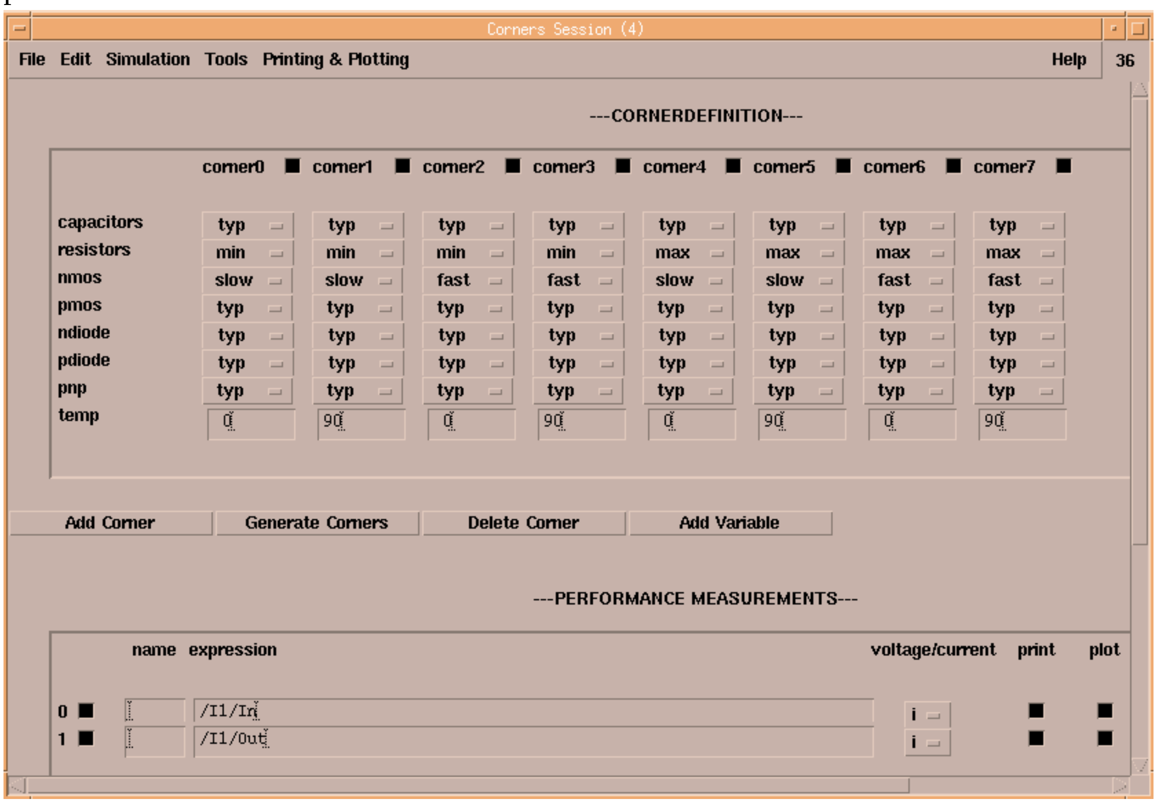
Press **OK** on the **Save Ocean Script to File** window then **Ok** on the **Start Corner Anlysis** window.



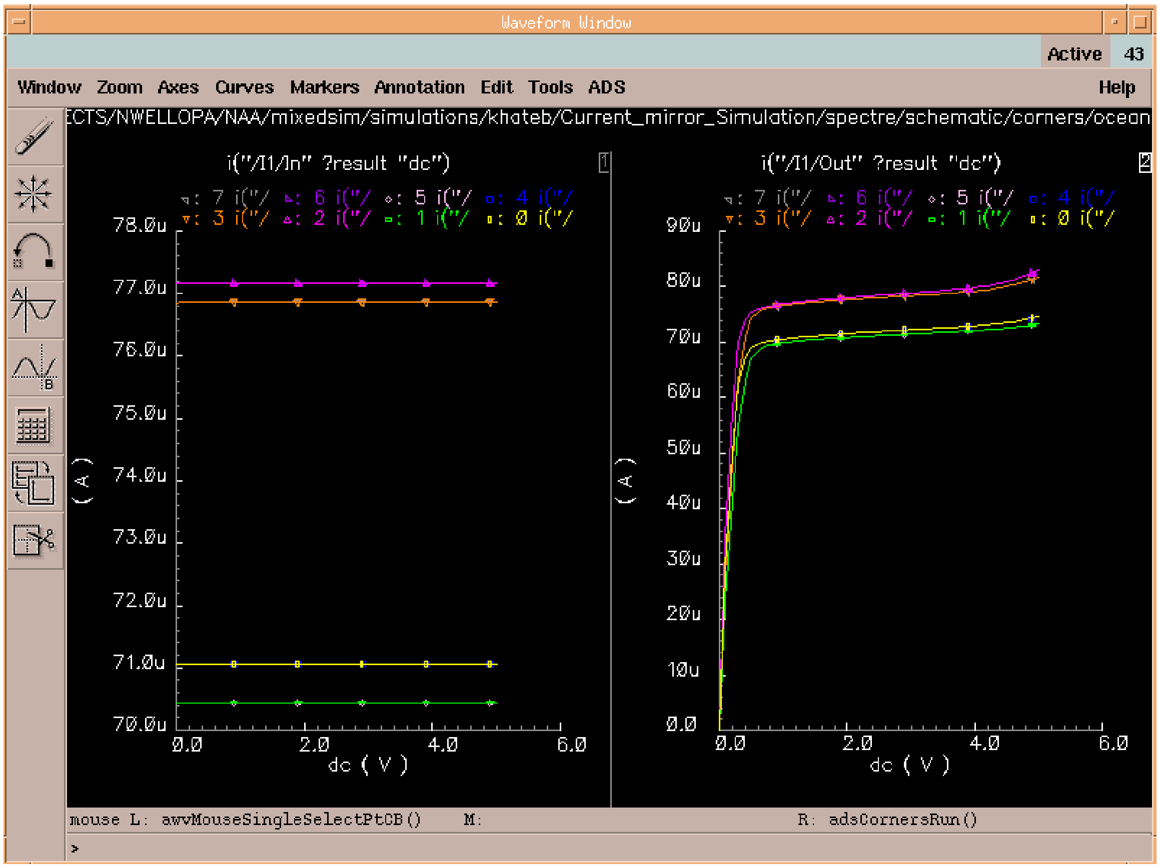
Choose **Add Variable** to add temperuter then press **Generat Corners**.



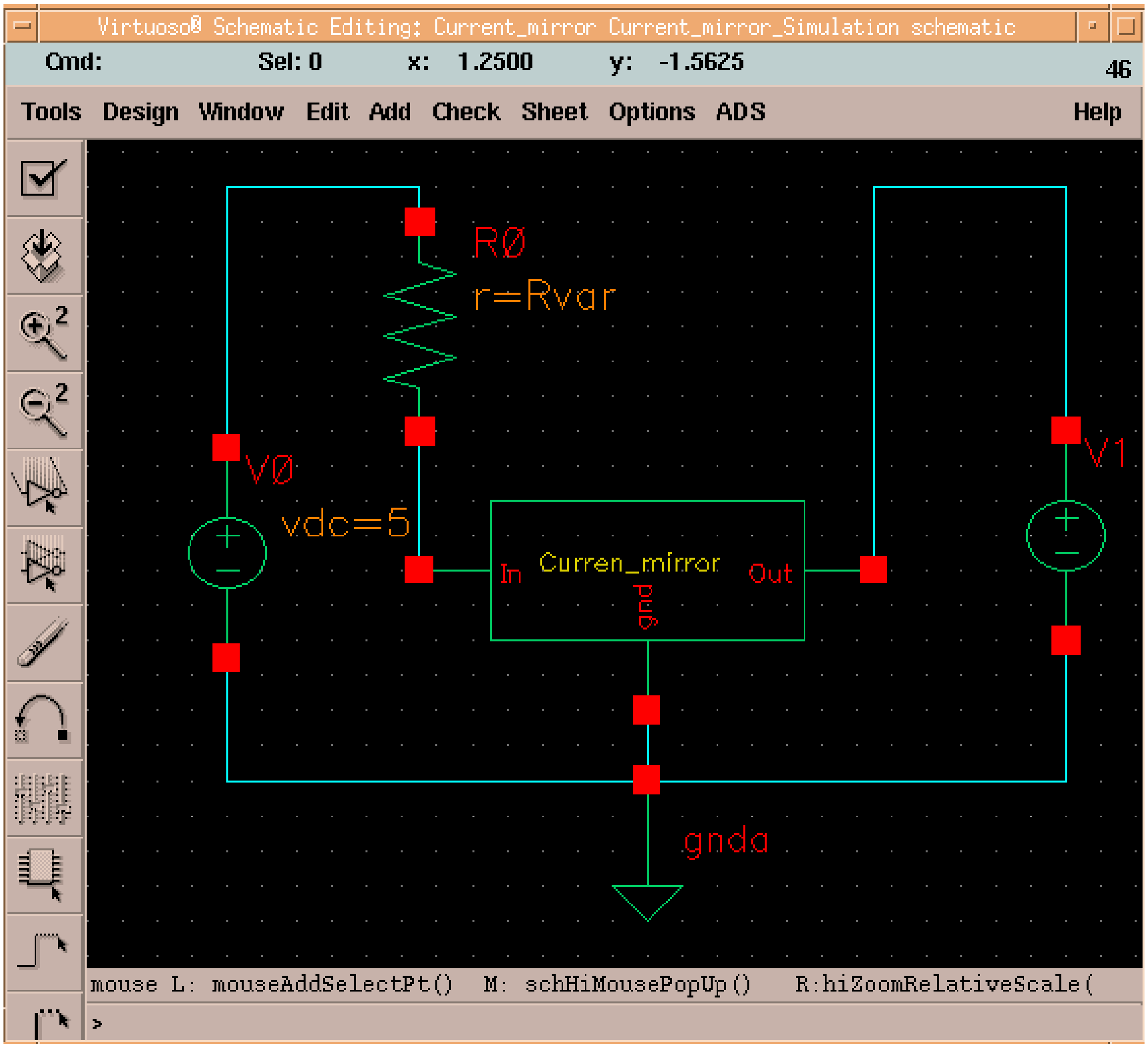
Now you can select one or more cases for each device and the temperature sweep then press **Generat Corners**.



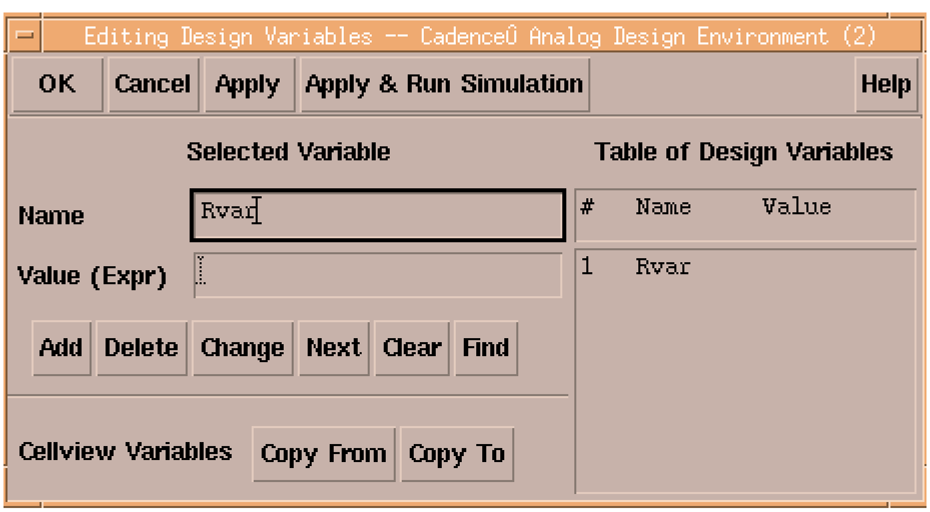
Press **Simulation** → **Run** then **OK**.



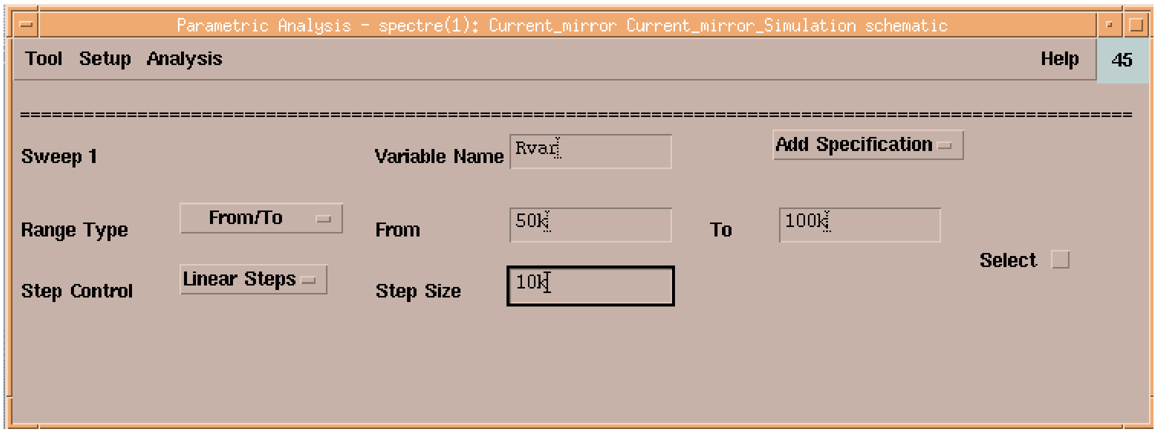
Parametric Analysis:
In **Virtuoso Schematic Editing** window, choose the instance for parametric analysis, for example **R0**, select **R0** press "**Q**" to open the **Edit Object Properties** window, on the **Resistance** filed type "**Rvar"** for example, press **OK** then **Check and Save**.



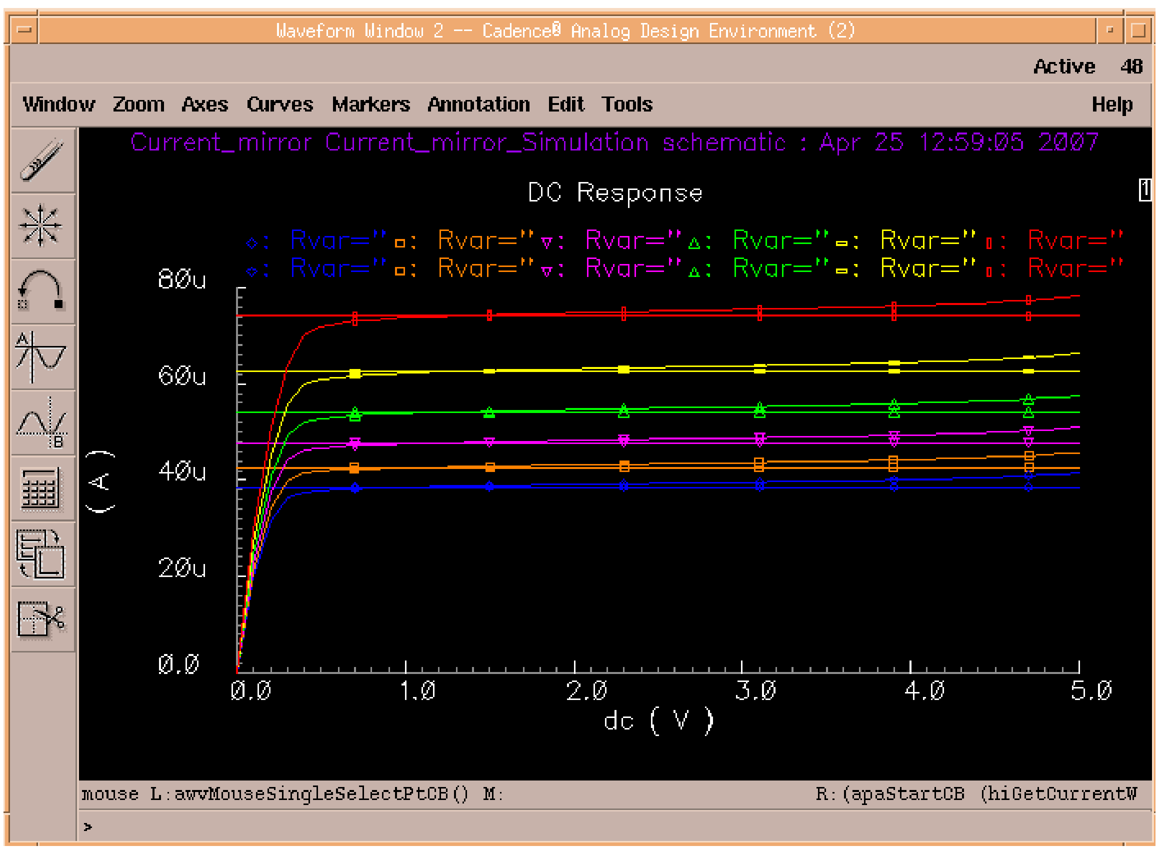
From the **Cadence Analog Design Environment** Simulation Window, Choose **Variable** → **Edit**…
In the **Editing Design Variable** window, type the name of the variable **Rvar**, press **OK**.



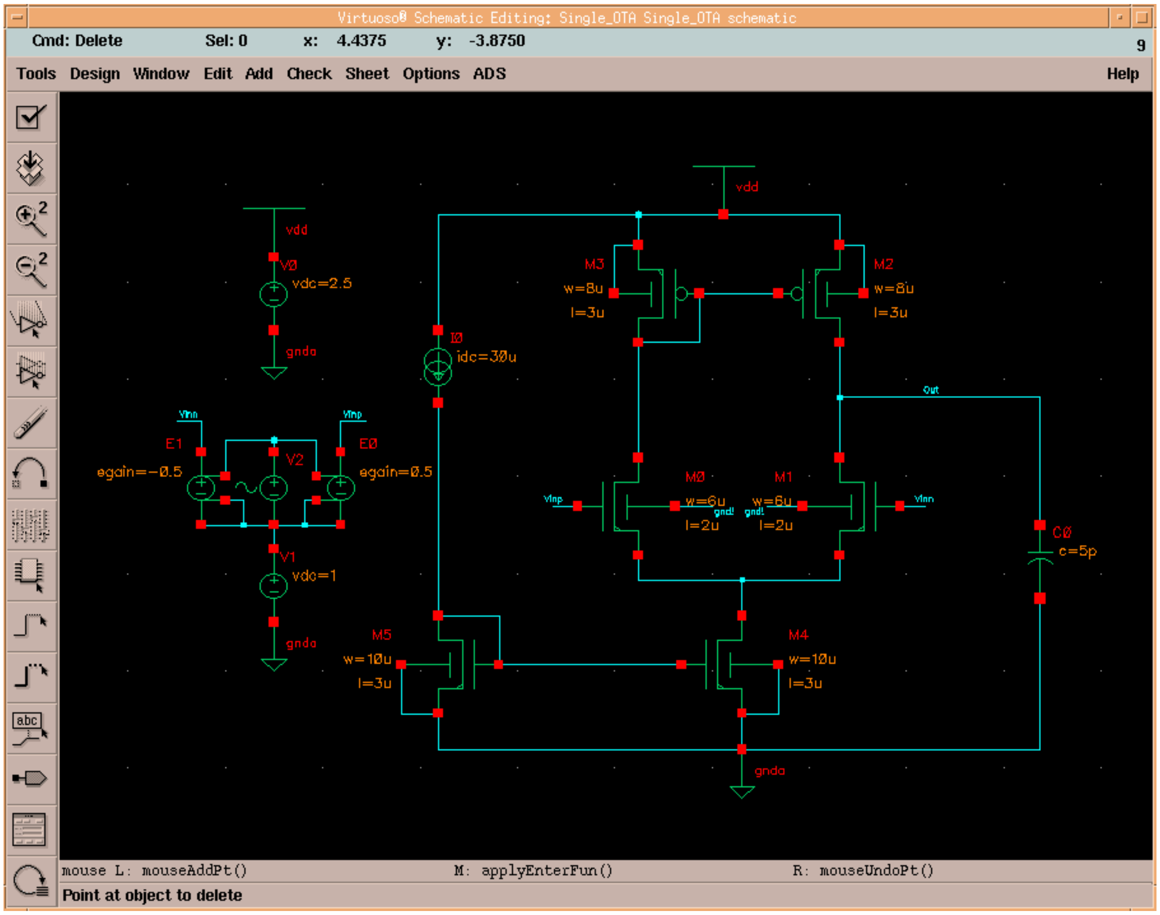
Now from the **Cadence Analog Design Environment** Simulation Window, Choose **Tools** → **Parametric Analysis…,** Parametric Analysis window appears. You use this window to specify values for the parametric analysis. You can enter many specifications, and you can choose options from three main menus at the top of the window. These menus are Tool, Setup, and Analysis.



From the **Parametric Analysis** Window, Choose **Analysis** → **Start**.



6.2 Single-ended Operational Transconductance Amplifier



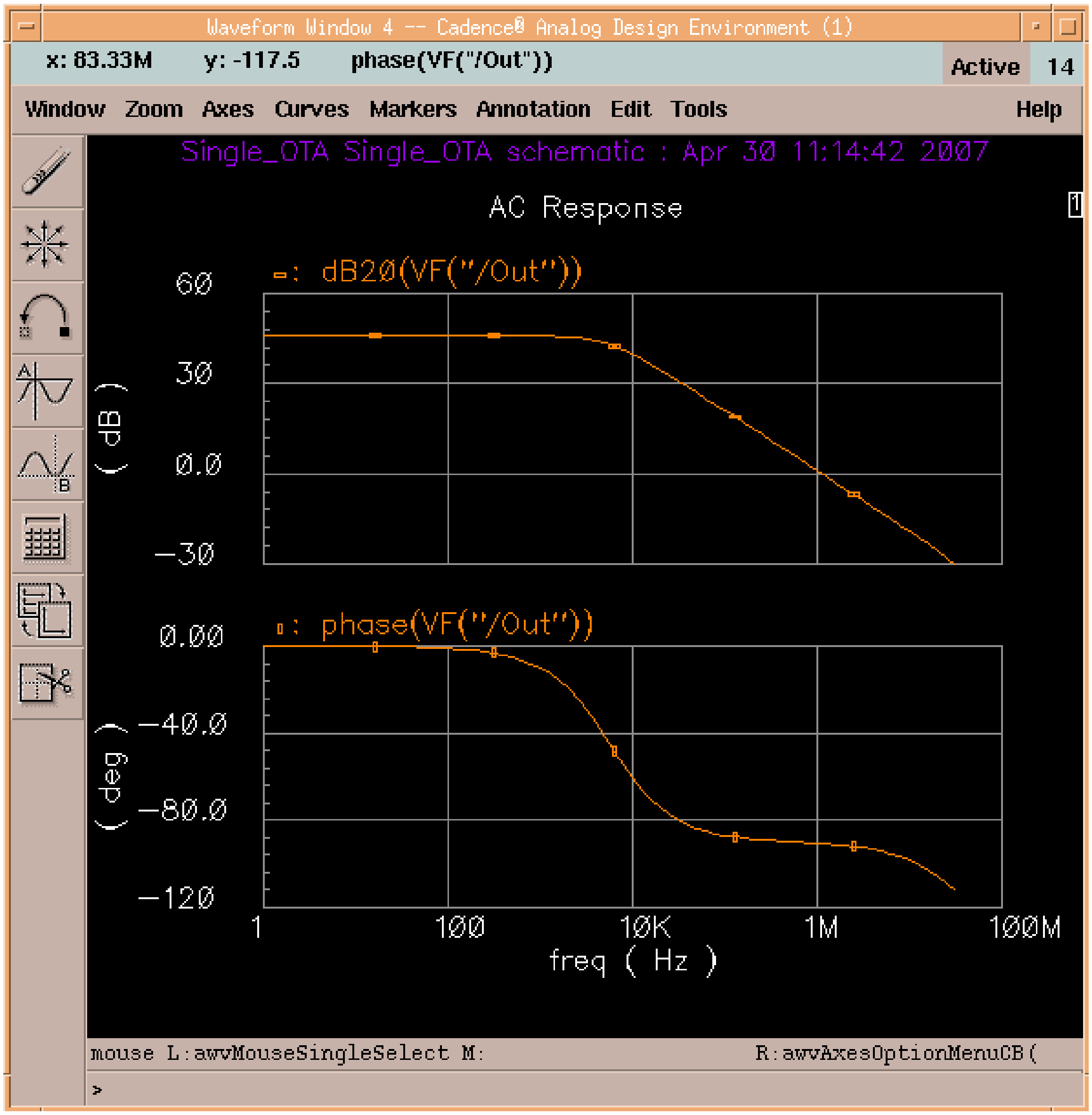
Signal source connection: Vdc=1V in series with a vsin, whose AC magnitude is 1V. Two vcvs are connected to the vsin. The gains are set to be 0.5 and -0.5 for vinp and vinn respectively.

DC Simulation

Run DC simulation and check the operating points (node voltage, branch current, transistor parameters). Fine tune the transistor size to meet the design specifications.

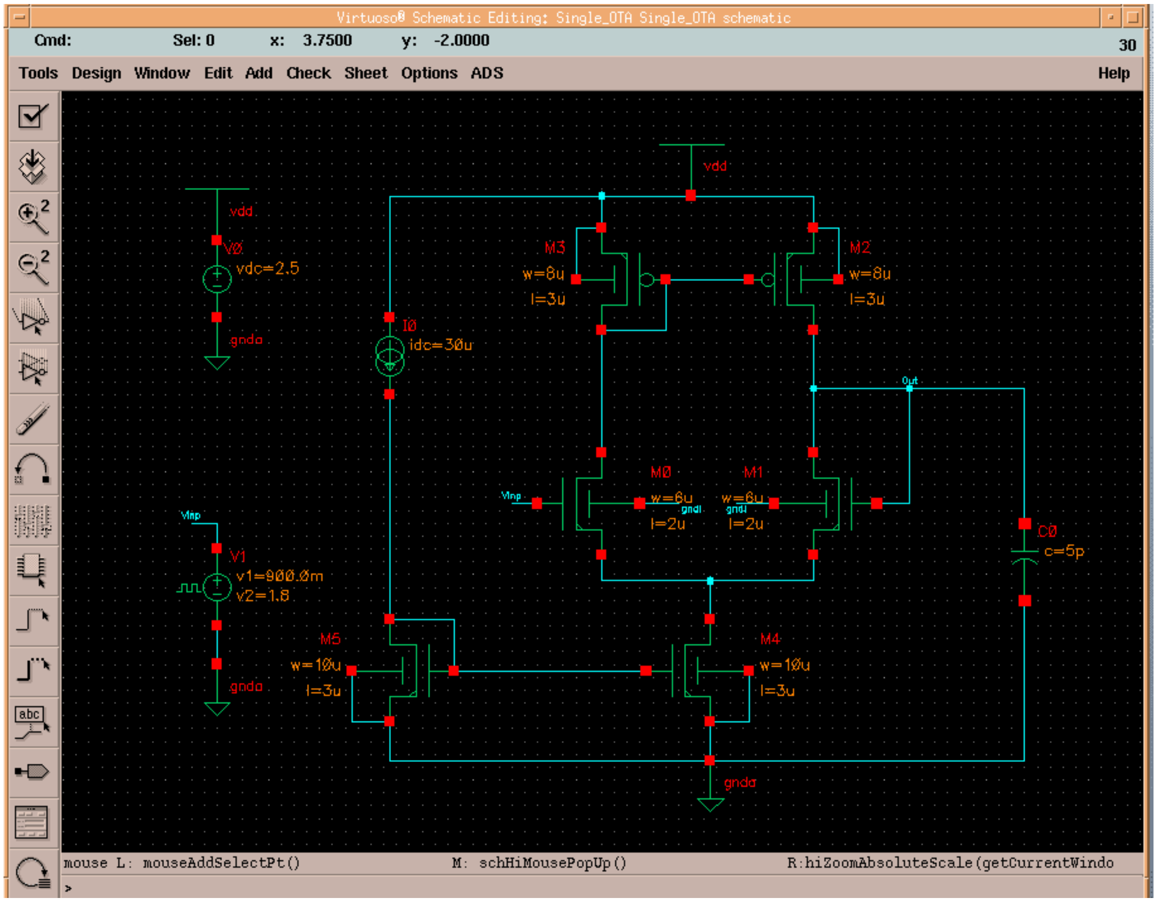
AC Simulation

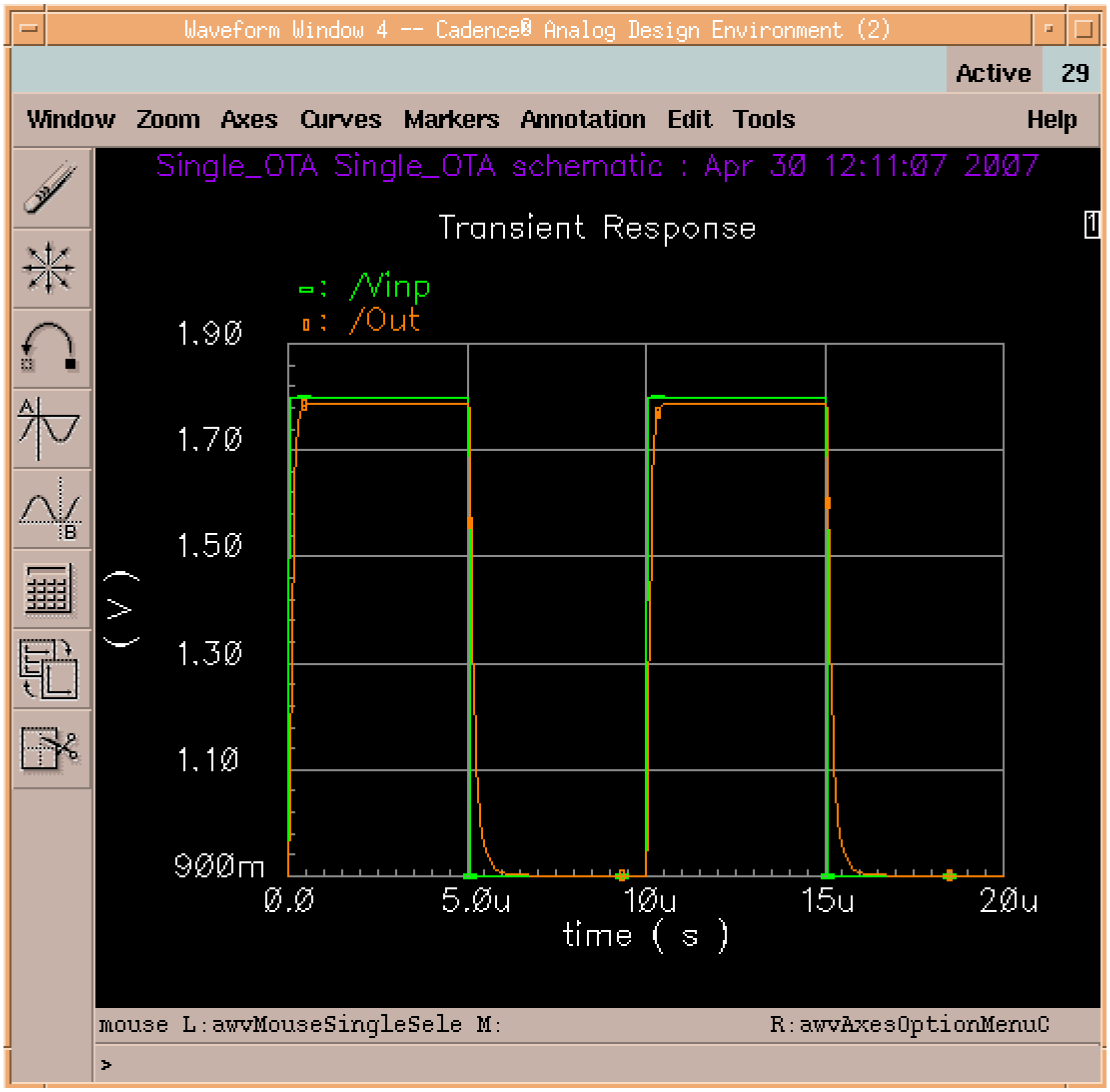
Set the AC simulation then run the simulation. When the simulation is successfully done, choose **Results** → **Direct Plot** → **AC Magnitude & Phase** in the **Analog Design Environment**. Then click on the wire connected to the top plate of the capacitor and press **Esc**. A Bode plot will show the AC response of the amplifier. Click on the “Switch Axis Mode” button to separate the plots.



Transient Response

Transient response is used to analyze the SR of the OTA. Connect the OTA as a voltage buffer. Apply a vpulse (0.9 -1.8V). The pulse period is set to be 10us and width is 5us. Run transient simulation, plot the output and measure the SR of both rising edge and falling edge.




Waveform Window 4 -- Cadence® Analog Design Environment (2)
Active 29
Window Zoom Axes Curves Markers Annotation Edit Tools Help
Single_OTA Single_OTA schematic : Apr 30 12:11:07 2007
Transient Response
/Vinp
/Out
1.90
1.70
1.50
1.30
1.10
900m
(V)
0.0
5.0u
10u
15u
20u
time (s)
mouse L:awvMouseSingleSele M:
R:awvAxesOptionMenuC

7 Reference

[1] Cadence Design Systems, Affirma™ Analog Circuit Design Environment User Guide
[2] Cadence Design Systems, Analog IC Design Tutorial for Schematic Design and Analysis using Spectre
[3] Cadence Design Systems, Waveform Calculator User Guide
[4] Cadence Design Systems, Virtuoso® Schematic Composer Tutorial
[5] Cadence Design Systems, Virtuoso® Advanced Analysis Tools User Guide
[6] Cadence Design Systems, Cadence SPICE™ Reference Manual
[7] Cadence Design Systems, Affirma RF Simulator User Guide
[8] Cadence Design Systems, Affirma™ Verilog®-A Language Reference
[9] AMS CMOS IC Design, Dr. Sameer Sonkusale